CHAPTER 10 TIME BASE COUNTER

The μPD70325 and 70335 each contain a long interval timer function for its watch function.

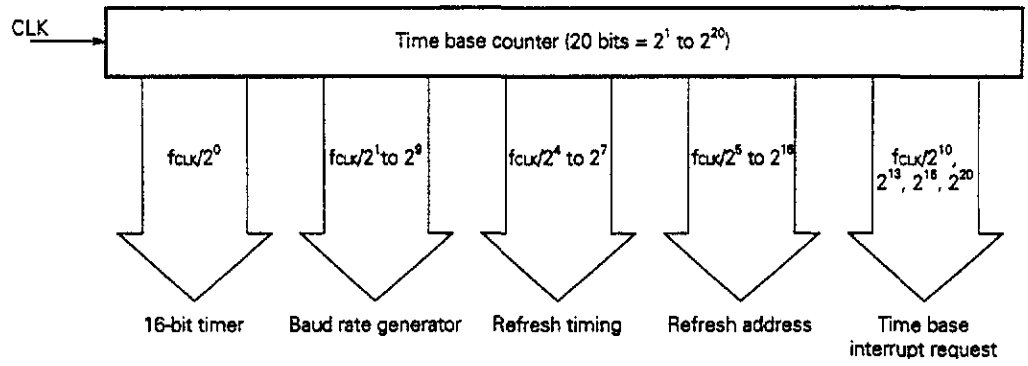
10.1 Time Base Counter Structure

Figure 10-1 shows the structure of the time base counter.

The time base counter consists of 20 frequency dividers that divide the system clock (CLK). The low-order part of the frequency divider tap output is used as a 16-bit timer count clock, a baud rate generator input clock, and for refresh timing generation and refresh address generation. Output taps at tap output bits 10, 13, 16, and 20 are used for time base interrupts.

When $\overline{\text{RESET}}$ is input, the time base counter contents are initialized to 00000H. After this, the time base counter continues to be incremented.

Figure 10-1. Time Base Counter Structure



10.2 Time Base Interval Specification

The interval time of an interrupt request occurring from the time base counter can be selected among the four types shown in Figure 10-2 by setting processor control register (PRC) bits 2 and 3 (TB0 and TB1).

Figure 10-2. PRC

7	6	5	4	3	2	1	0	When reset	R/W
0	RAMEN	0	0	TB1	TB0	PCK1	PCK0	4EH	R/W

When f_{CLK} = 8 MHz

TB1	TB0	Interval time
0	0	$2^{10}/f_{CLK}$ (128 μs)
0	1	$2^{13}/f_{CLK}$ (1.02 ms)
1	0	$2^{16}/f_{CLK}$ (8.19 ms)
1	1	$2^{20}/f_{CLK}$ (131 ms)

Caution The time immediately following setting of the TB0 and TB1 bits and until the first interrupt request occurs is undefined.

10.3 Time Base Interrupt Request Control Register (TBIC)

The TBIC register is an 8-bit register for mask control of interrupt requests occurring from the time base counter.

The TBIC register can be written/read by making an 8-bit or 1-bit memory access, in which case one wait state is inserted.

When $\overline{\text{RESET}}$ is input, the TBIC contents are initialized to 47H.

Figure 10-3. TBIC

7	6	5	4	3	2	1	0	When reset	R/W
TBF	TBMK	0	0	0	1	1	1	47H	R/W

When the time base counter output tap specified in the processor control register (PRC) goes high, the interrupt request flag (TBF) is set to 1, causing an interrupt request to occur.

TBIC bits 4 and 5 are fixed to 0. The time base counter interrupts do not support the register bank switching function or macro service function. TBIC bits 0 to 2 are fixed to 1 and the time base interrupt (INTTB) priority level is fixed to 7. It is fixed to the lowest priority level even when another interrupt having priority level "7" occurs. However, the time base interrupt is subjected to multiple servicing control.

[MEMO]