CHAPTER 7 PORT FUNCTIONS

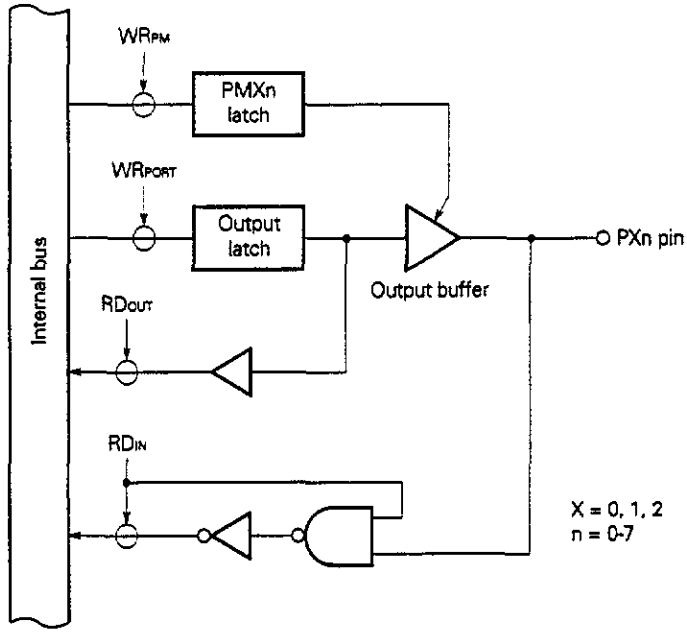
7.1 Ports 0 to 2

7.1.1 Hardware structure

Ports 0 to 2 in the μPD70325 and 70335 basically consist of three-state bidirectional ports such as shown in Figure 7-1.

When $\overline{\text{RESET}}$ is input, the port mode register bits are set to 1, specifying the input port mode. All of the port pins become high impedance. The output latch contents are not affected by $\overline{\text{RESET}}$ input.

Figure 7-1. Structure of Ports 0 to 2



Remark PMXn latch: port mode register PMX's bit n.

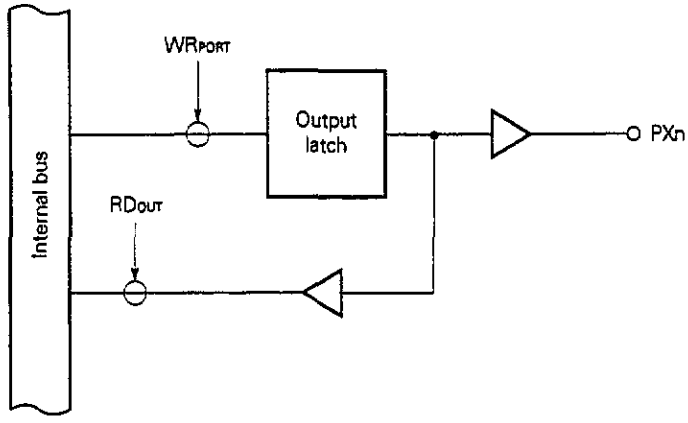
(1) When output port mode is specified (PMXn = 0)

The output latch becomes valid, and data can be transferred between the output latch and general-purpose register by executing a transfer instruction.

The output latch contents can be set as desired by executing a logical operation instruction. The data once written into the output latch is retained until a new port handling instruction is executed.

When reading port data, the output latch value is read rather than the output pin's state.

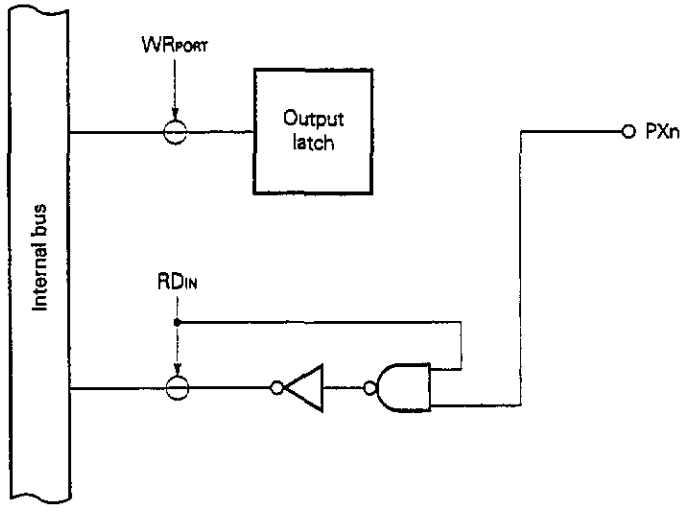
Figure 7-2. Port Set to Output Port Mode



(2) When input port is specified (PMXn = 1)

The port pin level can be loaded into the general-purpose register by executing a transfer instruction. In this case, data can be written into the output latch, and the data transferred from the general-purpose register by executing a transfer instruction is all stored in the output latch regardless of input or output port mode specification. However, since the output buffer of the bit set to the input port mode becomes high impedance, no output is made to the port pin. (When the bit set to the input port mode is changed to the output port mode, the output latch contents are output to the port pin.) The output latch contents of the bit set to the input port mode cannot be loaded into the general-purpose register.

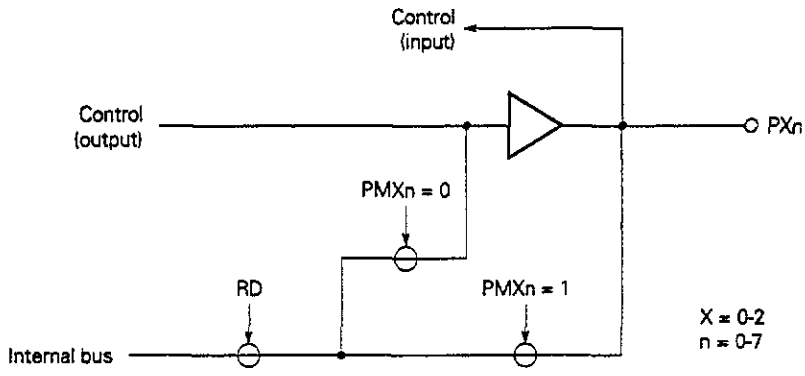
Figure 7-3. Port Set to Input Port Mode



(3) When control mode is specified (PMCXn = 1)

Ports 0 to 2 can be used as control signal input or output bit-wise by setting the port mode control register (PMCX) bits to 1 regardless of how the port mode register (PMX) is set. When using the pins as control signals, the control signal state can be read by executing a port access instruction.

Figure 7-4. Port Set to Control Mode



(a) When port is used as a control signal output

If a port read instruction is executed when the port mode register (PMXn) is set to 1, the control signal pin state can be read.

If a port read instruction is executed when the port mode register is reset to 0, the internal control signal state can be read.

(b) When port is used as control signal input

If a port read instruction is executed only when the port mode register is set to 1, the control signal pin state can be read.

7.1.2 Port functions

(1) P00 to P07 (port 0) - three-state input/output

Port 0 is an 8-bit special I/O port. It also functions as a system clock output pin (also used for P07) as well as a general purpose I/O port for which the input or output mode can be selected bit-wise. The function can be selected bit-wise by setting the port 0 mode register (PM0) and port 0 mode control register (PMC0).

Table 7-1. Operation of Port 0 (n = 0 to 7)

	PMC0n = 1	PMC0n = 0	
		PM0n = 1	PM0n = 0
P00	—	Input port	Output port
P01		Input port	Output port
P02		Input port	Output port
P03		Input port	Output port
P04		Input port	Output port
P05		Input port	Output port
P06		Input port	Output port
P07	CLKOUT output	Input port	Output port

(a) Port 0 mode control register (PMC0)

The port 0 mode control register (PMC0) is an 8-bit register that selects the port or system clock output mode bit-wise for port 0. This register can only be written by making an 8-bit memory access. If the corresponding bit of the PMC0 register is set to 1, the system clock output mode (P07) is selected; if it is reset to 0, the port mode is selected.

When $\overline{\text{RESET}}$ is input, all of the PMC0 register bits are reset to 0, selecting the port mode.

Figure 7-5. PMC0

7	6	5	4	3	2	1	0	When reset	R/W
PMC0 7	0	0	0	0	0	0	0	00H	W

0	P0n = port mode
1	P07 = system clock output

(b) Port 0 mode register (PM0)

The port 0 mode register (PM0) is an 8-bit register that selects the input or output mode bit-wise for port 0. This register can only be written by making an 8-bit memory access. When the corresponding bit of PMC0 is 0, PM0 becomes valid.

When $\overline{\text{RESET}}$ is input, all of the PM0 bits are set to 1 and port 0 becomes an input port.

Figure 7-6. PM0

7	6	5	4	3	2	1	0	When reset	R/W
PMC0	PM0	PM0	PM0	PM0	PM0	PM0	PM0	FFH	W
7	6	5	4	3	2	1	0		

PMC0	0	P0n = output
=0	1	P0n = input

(n = 0-7)

(2) P10 to P17 (port 1) - three-state input/output

Port 1 is an 8-bit special I/O port. It also functions as various control pins as well as a general purpose I/O port for which the input or output mode can be selected bit-wise like port 0. The function can be selected bit-wise by setting the port 1 mode register (PM1) and port 1 mode control register (PMC1).

The pin levels for P10 to P13 can be read by directly reading port 1 (P1).

The P10 pin cannot be used as a general-purpose input port.

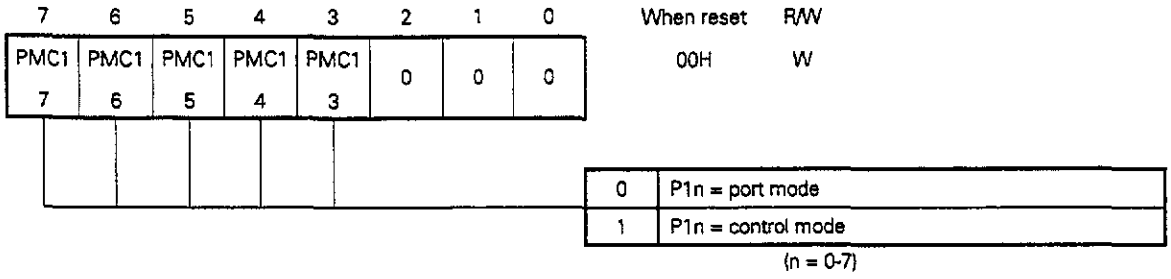
Table 7-2. Operation of Port 1 (n = 0 to 7)

	PMC1n = 1	PMC1n = 0	
		PM1n = 1	PM1n = 0
P10	—	NMI input	—
P11		$\overline{\text{INTP0}}$ input	
P12		$\overline{\text{INTP1}}$ input	
P13	$\overline{\text{INTAK}}$ output	$\overline{\text{INTP2}}$ input	
P14	INT input	Input port ($\overline{\text{POLL}}$ input)	Output port
P15	TOUT output	Input port	Output port
P16	$\overline{\text{SCK0}}$ output	Input port	Output port
P17	READY input	Input port	Output port

(a) Port 1 mode control register (PMC1)

The port 1 mode control register (PMC1) is an 8-bit register that selects the port or control signal input/output mode bit-wise for port 1. This register can only be written by making an 8-bit memory access. If the corresponding bit of the PMC1 register is set to 1, the control signal input/output mode is selected; if it is reset to 0, the port mode is selected. When $\overline{\text{RESET}}$ is input, all PMC1 register bits are reset to 0, selecting the port mode. However, P10 to P12 are fixed to the port mode.

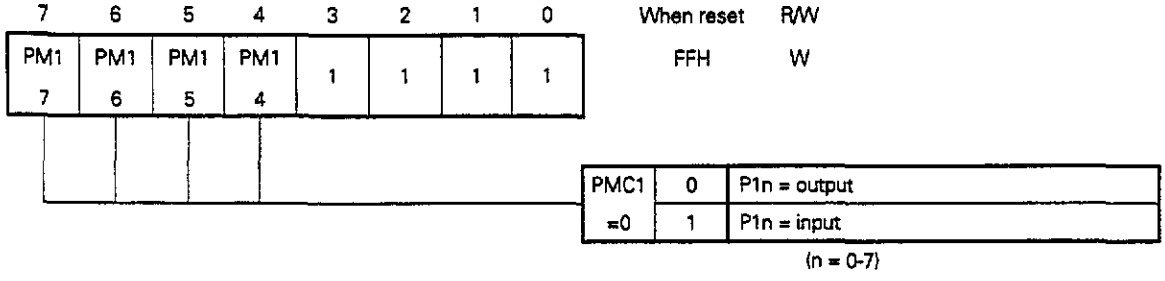
Figure 7-7. PMC1



(b) Port 1 mode register (PM1)

The port 1 mode register (PM1) is an 8-bit register that selects the input or output mode bit-wise for port 1. This register can only be written by making an 8-bit memory access. When the corresponding bit of the PMC1 register is set to 0, PM1 becomes valid. When $\overline{\text{RESET}}$ is input, all the PM1 bits are set to 1, selecting the input mode.

Figure 7-8. PM1



(3) P20 to P27 (port 2) - three-state input/output

Port 2 is an 8-bit special I/O port. It also functions as various control pins as well as a general purpose I/O port for which the input or output mode can be selected bit-wise like port 0. The function can be selected bit-wise by setting the port 2 mode register (PM2) and port 2 mode control register (PMC2).

Table 7-3. Operation of Port 2 (n = 0 to 7)

	PMC2n = 1	PMC2n = 0	
		PM2n = 1	PM2n = 0
P20	DMARQ0 input	Input port	Output port
P21	$\overline{\text{DMAAK0}}$ input	Input port	Output port
P22	$\overline{\text{TC0}}$ output	Input port	Output port
P23	DMARQ1 input	Input port	Output port
P24	$\overline{\text{DMAAK1}}$ output	Input port	Output port
P25	$\overline{\text{TC1}}$ output	Input port	Output port
P26	$\overline{\text{HLDAK}}$ output	Input port	Output port
P27	HLDRQ input	Input port	Output port

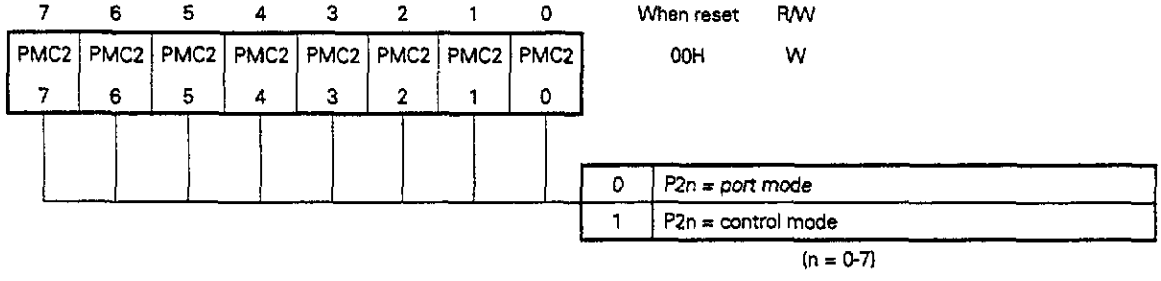
(a) Port 2 mode control register (PMC2)

The port 2 mode control register (PMC2) is an 8-bit register that selects the port or control signal input/output mode bit-wise for port 2.

This register can only be written by making an 8-bit memory access.

If the corresponding bit of the PMC2 register is set to 1, the control signal input/output mode is selected; if it is reset to 0, the port mode is selected. When $\overline{\text{RESET}}$ is input, all PMC2 register bits are reset to 0, selecting the port mode.

Figure 7-9. PMC2



(b) Port 2 mode register (PM2)

The port 2 mode register (PM2) is an 8-bit register that selects the input or output mode bit-wise for port 2. This register can only be written by making an 8-bit memory access.

When the corresponding bit of the PMC2 register is set to 0, the various PM2 bits become valid.

When $\overline{\text{RESET}}$ is input, all of the PM2 bits are set to 1, selecting input mode.

Figure 7-10. PM2

7	6	5	4	3	2	1	0	When reset	R/W
PM2 7	PM2 6	PM2 5	PM2 4	PM2 3	PM2 2	PM2 1	PM2 0	FFH	W

PMC2 =0	0	P2n = output
	1	P2n = input

(4) Cautions

The following cautions should be observed when using the above pins as output ports after a reset is input.

- **Power-on reset**

  Because the contents of the output latch are undefined, when using these pins as an output port, first write the values to be output to the port, then switch the port mode register from input mode to output mode.

  If the mode is switched before setting the port, undefined values will be output from the port pins.

- **System reset**

  Because the output latch value prior to reset is retained, switching the port mode register from input mode to output mode causes the output latch value prior to reset to be output from the port pins.

7.2 Port T (PT0 to PT7)

Port T is an 8-bit input port that enables the threshold voltage (reference voltage) to be changed among 16 stages. Comparator operation is performed according to the analog input.

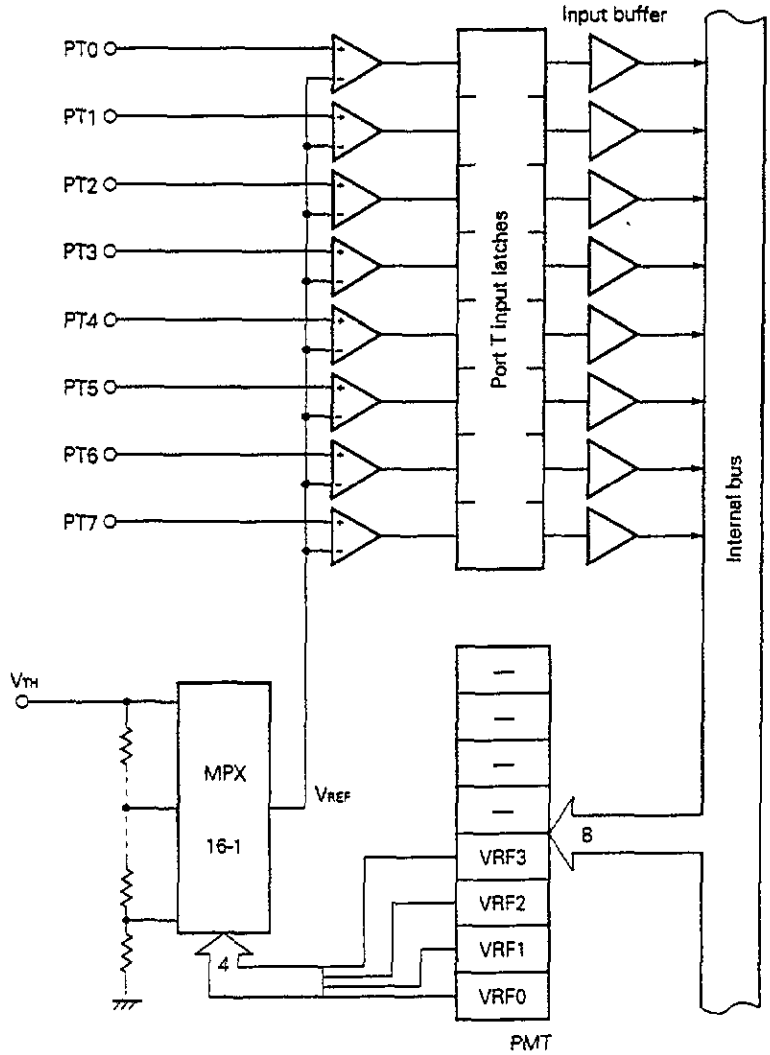
7.2.1 Hardware structure

Port T consists of comparator input for PT0 to PT7, the V_{TH} pin (reference voltage input), the multiplexer (MPX) that selects the comparison voltage (V_{REF}) among 16 types (from 1/16 × V_{TH} to 16/16 × V_{TH}), the port mode T register (PMT) that controls the MPX, and eight latches, as shown in Figure 7-11.

The comparator compares V_{REF}, selected by setting PMT, with PT0 to PT7 input and the result is latched in the port T input latches.

$$\begin{cases} V_{REF} > PTn \rightarrow 0 \\ V_{REF} < PTn \rightarrow 1 \end{cases}$$

Figure 7-11. Block Diagram of Port T



Caution The V_{TH} pin is connected via high resistance to the GND pin. Therefore, if voltage is applied to the V_{TH} pin in the standby mode, the consumption current will increase.

7.2.2 Port T mode register (PMT)

The port T mode register (PMT) is an 8-bit register that selects the comparator's comparison voltage (V_{REF}) among the 16 types shown in Figure 7-12.

This register can be written/read by making an 8-bit or 1-bit memory access.

When $\overline{RESET}$ is input, all of the PMT bits are reset to 0.

Figure 7-12. PMT

7	6	5	4	3	2	1	0	When reset	R/W
-	-	-	-	VREF 3	VREF 2	VREF 1	VREF 0	00H	R/W

VREF 3	VREF 2	VREF 1	VREF 0	V_{REF}
0	0	0	0	$V_{TH} \times 16/16$
0	0	0	1	$V_{TH} \times 1/16$
0	0	1	0	$V_{TH} \times 2/16$
0	0	1	1	$V_{TH} \times 3/16$
0	1	0	0	$V_{TH} \times 4/16$
0	1	0	1	$V_{TH} \times 5/16$
0	1	1	0	$V_{TH} \times 6/16$
0	1	1	1	$V_{TH} \times 7/16$
1	0	0	0	$V_{TH} \times 8/16$
1	0	0	1	$V_{TH} \times 9/16$
1	0	1	0	$V_{TH} \times 10/16$
1	0	1	1	$V_{TH} \times 11/16$
1	1	0	0	$V_{TH} \times 12/16$
1	1	0	1	$V_{TH} \times 13/16$
1	1	1	0	$V_{TH} \times 14/16$
1	1	1	1	$V_{TH} \times 15/16$

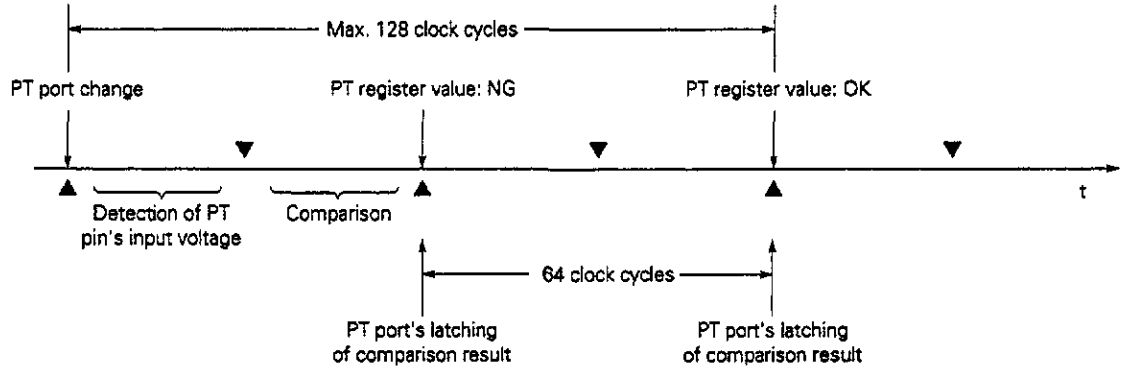
7.2.3 Port T reception

The comparison operation for PT0 to PT7 is executed in the following two stages.

First stage : PT pin voltage is detected.
Second stage : voltage detected at first stage is compared with voltage set by PMT register.

The comparison period, which is the sum of the execution times for the first and second stages, is 64 clocks.

The first and second stages are always executed alternately. The start timing cannot be controlled by software or hardware. Therefore, to obtain an accurate comparison result after the PT pin's input voltage or comparison voltage has been changed, wait until 128 clock cycles have elapsed before reading the PT register value. During this period, make sure that the PT pin's input voltage is stable.



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