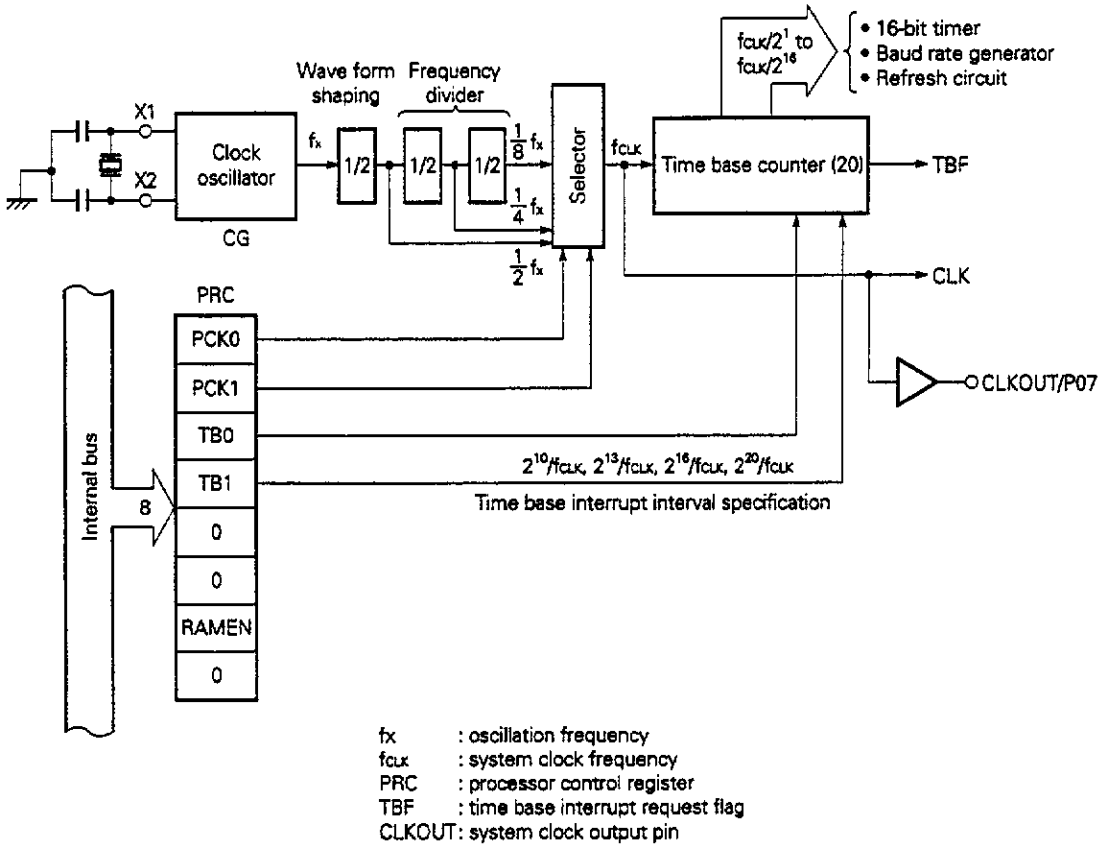
CHAPTER 8 CLOCK GENERATOR

The clock generator supplies various clocks to the CPU and peripheral hardware and also controls the CPU operation mode.

8.1 Clock Generator Structure

Figure 8-1 shows a block diagram of the clock generator.

Figure 8-1. Block Diagram of Clock Generator



fx : oscillation frequency
fCLK : system clock frequency
PRC : processor control register
TBF : time base interrupt request flag
CLKOUT: system clock output pin

The clock generator clock oscillates using a crystal or ceramic resonator connected to the X1 and X2 pins.

The clock oscillator output frequency is divided by two for wave form shaping. The dividing ratio is selected for use as a system clock (CLK).

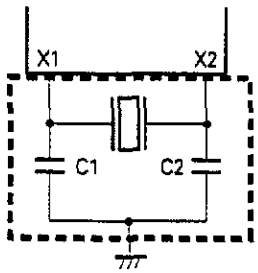
The CLK dividing ratio can be selected among 1/2, 1/4, and 1/8 of the oscillation frequency (fx) by setting processor control register (PRC) bits 0 and 1 (PCK0 and PCK1).

As CLK is set to low speed, the system clock frequency becomes low, and long operation is possible even when the voltage is lowered in a battery-driven system.

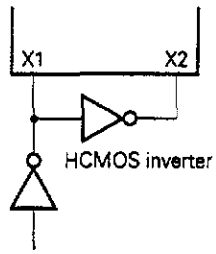
External clocks can also be input.

Figure 8-2. Clock Generator External Circuit

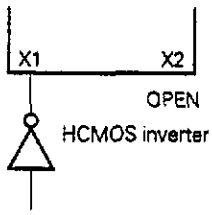
(a) Crystal or ceramic oscillation



(b) External clock input



(c) External clock input (X2: open)



Cautions 1. Put the external components as close as possible to the X1 and X2 pins.

2. Do not pass any other signal through the area indicated with dotted lines.

Table 8-1. Recommended Ceramic Resonators

Manufacturer	Product name	Recommended constants	
		C1 [pF]	C2 [pF]
Murata	CSA16.00MX040	30	30
	CSA20.00MX040	10	10
TDK	FCR16.0M2G	30	30

Table 8-2. Recommended Crystal Resonators

Manufacturer	Product name	Recommended constants	
		C1 [pF]	C2 [pF]
Kinseki	HC-49/U (KR-100)	22	22
	HC-49/U (KR-160)	22	22
	HC-49/U (KR-200)	22	22

Remark Be sure to check with the resonator manufacturer regarding resonator characteristics, etc.

8.2 Processor Control Register (PRC)

The processor control register (PRC) is an 8-bit register that controls CPU and internal system control items such as the CPU operation clock, time base interrupt intervals, and enabling of internal RAM memory references.

This register can be written/read by making an 8-bit or 1-bit memory access.

When $\overline{\text{RESET}}$ is input, the PRC contents are initialized to 4EH.

The system clock dividing ratio is specified by setting the PCK0 and PCK1 bits. The oscillation frequency is divided by the value specified in PCK0 and PCK1, and the result is used as the system clock (CLK).

The time base interrupt intervals are specified by setting the TB0 and TB1 bits. One of four long interval time types can be selected in the TB0 and TB1 bits.

Enabling of internal RAM memory references is controlled by setting the RAMEN bit. When the RAMEN bit is set to 0 (memory reference disable), address judgment of internal RAM is not made and external memory is always accessed.

When RAM is referenced as a register, internal RAM is always accessed.

Figure 8-3. PRC

7	6	5	4	3	2	1	0	When reset	R/W
0	RAMEN	0	0	TB1	TB0	PCK1	PCK0	4EH	R/W

PCK1	PCK0	System clock (CLK) dividing ratio specification
0	0	f_{CLK} = oscillation frequency (fx) x 1/2
0	1	f_{CLK} = oscillation frequency (fx) x 1/4
1	0	f_{CLK} = oscillation frequency (fx) x 1/8
1	1	Setting prohibited

TB1	TB0	Time base interrupt interval specification
0	0	Interrupt generation at intervals of $2^{10}/f_{CLK}$
0	1	Interrupt generation at intervals of $2^{13}/f_{CLK}$
1	0	Interrupt generation at intervals of $2^{15}/f_{CLK}$
1	1	Interrupt generation at intervals of $2^{20}/f_{CLK}$

RAMEN	Internal RAM enable specification
0	Internal RAM disable
1	Internal RAM enable