CHAPTER 1 GENERAL DESCRIPTION

The μPD70325 and 70335 (or V25+ and V35+, respectively) are microcontrollers with partially improved peripheral functions of the single-chip microcontrollers μPD70320 and 70330 (or V25 and V35, respectively), and are software-compatible with the μPD70108 and 70116 (or V20 and V30, respectively).

Both of μPD70325 and 70335 (or V25+ and V35+, respectively) contain a 16-bit CPU. The V25 has an 8-bit external data bus and the V35 has a 16-bit external data bus.

The μPD70325 and 70335 (or V25+ and V35+, respectively) feature, like the μPD70320 and 70330 (or V25 and V35, respectively), powerful interrupt functions that are important for control applications. In addition, their on-chip peripheral functions include an interval timer, serial interface, and high-speed DMA controller.

Original user-friendly architectures such as a memory-mapped register bank, on-chip hardware, etc. have also been adopted while maintaining their software-compatible ability.

Based on these features, both of these products are applicable as main controllers in systems where large amounts of data are processed and many devices are controlled. In particular, these devices are applicable for controlling systems that handle mass data and devices such as printers, word processors, and other terminals.

1.1 Features

- o Internal 16-bit architecture
- o External data bus width
  - μPD70325: 8 bits
  - μPD70335: 16 bits
- o Software compatible with μPD70108, 70116 in native mode (additional instructions are provided)
- o 3-stage pipeline system
- o Minimum instruction cycle
  - μPD70325-8, 70335-8 : 250 ns (with external clock of 16 MHz)
  - μPD70325(A)-9, 70335(A)-9: 220 ns (with external clock of 18 MHz)
  - μPD70325-10, 70335-10 : 200 ns (with external clock of 20 MHz)
- o Internal memory RAM: 256 bytes
- o Memory space: 1 Mbyte
- o I/O space: 64 Kbytes
- o Register banks (memory-mapped): 8 banks
- o On-chip peripheral hardware mapped in memory (special function registers)
- o Input port with comparator (port T): 8 bits
- o I/O lines Input port: 4 bits
  I/O ports: 20 bits
- o Serial interface: 2 channels
  - On-chip dedicated baud rate generator
  - Asynchronous mode, I/O interface mode
- o Interrupt controller
  - Eight programmable priority levels
  - Three interrupt response modes
    Vectored interrupt function
    Register bank switching function
    Macro service function
- o DRAM, pseudo SRAM refresh function
- o DMA controller: 2 channels
  - Four DMA transfer modes
  - Transfer rate
    μPD70325-8 : Max. 4 MB/s[Note 1] or Max. 2 MB/s[Note 2]
    μPD70325-10: Max. 5 MB/s[Note 1] or Max. 2.5 MB/s[Note 2]
    μPD70335-8 : Max. 5.3 MB/s[Note 1] or Max. 2.7 MB/s[Note 2]
    μPD70335-10: Max. 6.7 MB/s[Note 1] or Max. 3.3 MB/s[Note 2]
- o 16-bit timer: 2 channels
- o Time base counter (20 bits): 1 channel
- o Programmable wait function
- o Standby function (STOP or HALT)
- o CMOS
- o Packages
  - 84-pin plastic QFJ (Quad Flat J-leaded Package)
  - 94-pin plastic QFP (Quad Flat Package)
- o The μPD70325 (A) and 70335 (A) feature a wider operating temperature range in comparison with the μPD70325 and 70335.

Notes 1. Demand release mode (for not stop control by DMARQ pin)
2. Demand release mode (for stop control by DMARQ pin) or burst mode

1.2 Differences with V25 and V35

		V25	V35	V25+	V35+
		μPD70320	μPD70330	μPD70325	μPD70335
DMA function	Transfer processing method	Microprogram		Dedicated hardware	
	Maximum transfer rate (@ 8 MHz)	0.6 Mbytes/s	0.8 Mbytes/s	4 Mbytes/s	5.3 Mbytes/s
	DMA request sampling timing	Between instruction execution cycles		Between bus cycles	
	DMA service channel	In on-chip RAM area		In special function register area	
	Transfer address specification method	Segment		Linear	
	Execution form in single step mode	One DMA transfer/one instruction execution		One DMA transfer/one bus cycle	
	Interrupt request during DMA transfer (demand release mode)	Only NMI is acknowledged		Not acknowledged	
	No. of required wait cycles for DMARQ stop control (demand release mode)	Not required		Two wait cycles	
	Transfer processing units	Bytes or words	Bytes or words	Bytes	Bytes or words
	TC (Terminal Counter) setup value	DMA transfer count		(DMA transfer count) - 1	
	Terminal count generation timing	TC=0		TC=FFFFH	
	TC output low level width	Fixed		Widened by wait insertion	
Serial interface	Transmission clock output (channel 0) in asynchronous mode	Disabled		Enabled ($\overline{SCK0}$ pin)	
	Serial error register	Available		Serial status register	
	Receive buffer full flag	Not available		In serial status register	
	Transmit buffer empty flag	Not available		In serial status register	
	All sent flag	Not available		In serial status register	
Interrupt function	Interrupt cause register	Not available		Available	
Maximum operation frequency		8 MHz		10 MHz	

1.3 Ordering Information and Quality Grade

(1) Ordering Information

Part number	External data bus (bits)	Package	Maximum operation frequency (MHz)
μPD70325L-8	8	84-pin plastic QFJ	8
μPD70325L-10	8	84-pin plastic QFJ	10
μPD70325GJ-8-5BG	8	94-pin plastic QFP	8
μPD70325GJ-10-5BG	8	94-pin plastic QFP	10
μPD70335L-8	16	84-pin plastic QFJ	8
μPD70335L-10	16	84-pin plastic QFJ	10
μPD70335GJ-8-5BG	16	94-pin plastic QFP	8
μPD70335GJ-10-5BG	16	94-pin plastic QFP	10
μPD70325GJ(A)-9-5BG	8	94-pin plastic QFP	9
μPD70335GJ(A)-9-5BG	16	94-pin plastic QFP	9

QFJ: Quad Flat J-leaded Package
QFP: Quad Flat Package

(2) Quality Grade

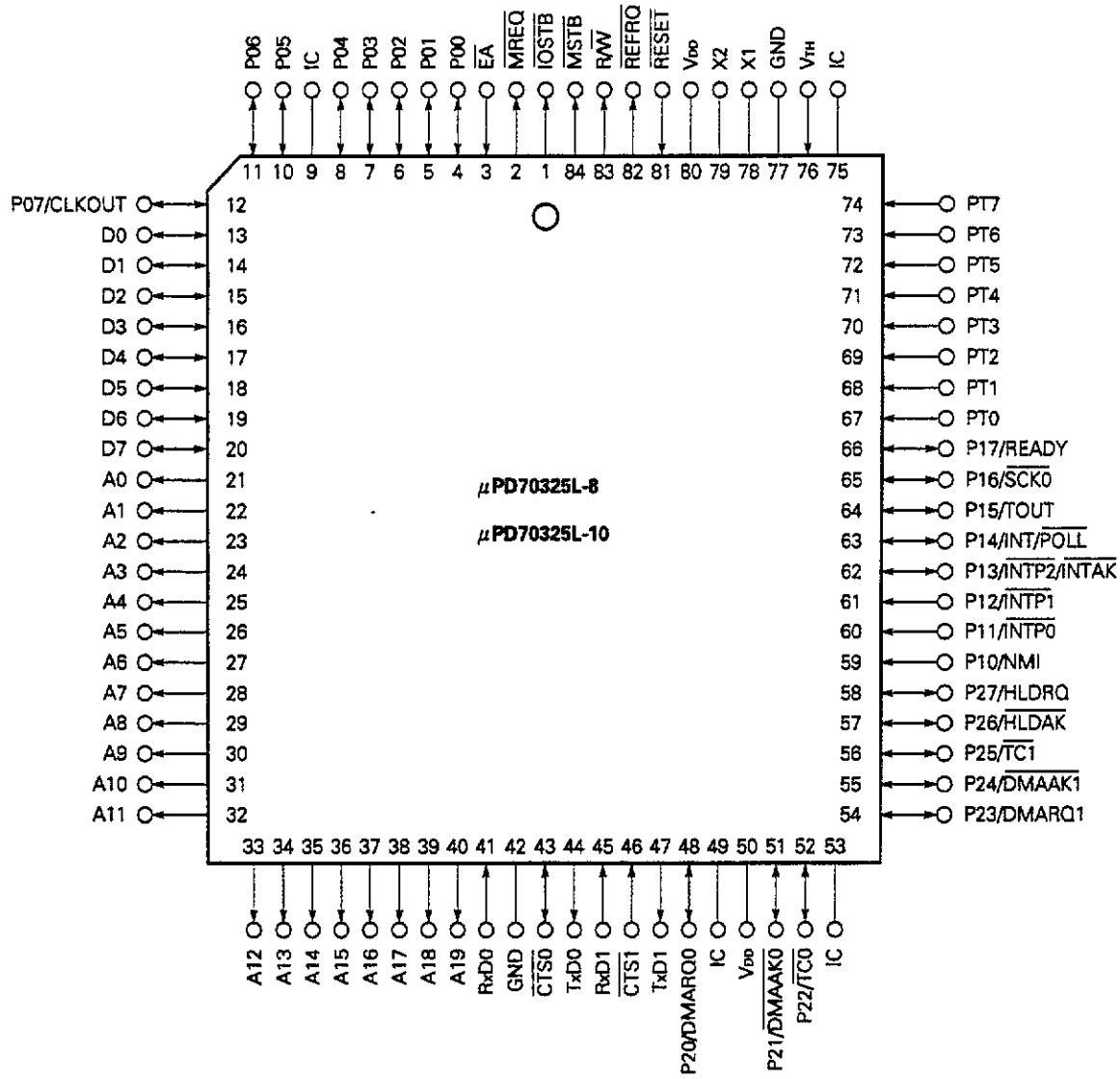
Part number	Package	Quality grade
μPD70325L-8	84-pin plastic QFJ	Standard
μPD70325L-10	84-pin plastic QFJ	Standard
μPD70325GJ-8-5BG	94-pin plastic QFP	Standard
μPD70325GJ-10-5BG	94-pin plastic QFP	Standard
μPD70335L-8	84-pin plastic QFJ	Standard
μPD70335L-10	84-pin plastic QFJ	Standard
μPD70335GJ-8-5BG	94-pin plastic QFP	Standard
μPD70335GJ-10-5BG	94-pin plastic QFP	Standard
μPD70325GJ(A)-9-5BG	94-pin plastic QFP	Special
μPD70335GJ(A)-9-5BG	94-pin plastic QFP	Special

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

1.4 Pin Configuration (Top View)

(1) 84-pin plastic QFJ

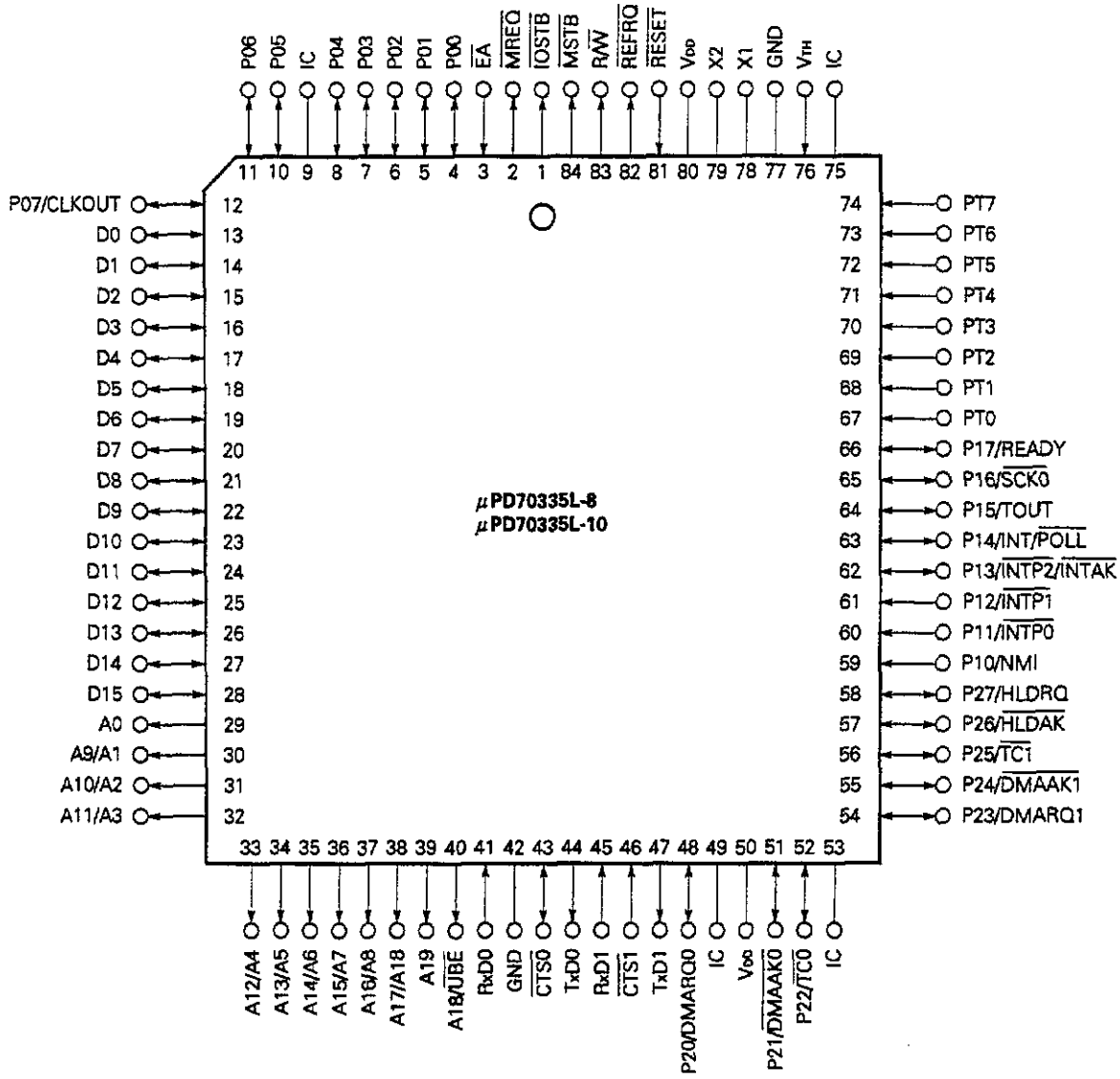
(a) μPD70325



IC : Internally Connected

Cautions 1. Connect each IC pin to V_{DD} individually via a resistor (3 to 10 kΩ).
2. Connect the $\overline{EA}$ pin to GND via a resistor (3 to 10 kΩ).

(b) μPD70335

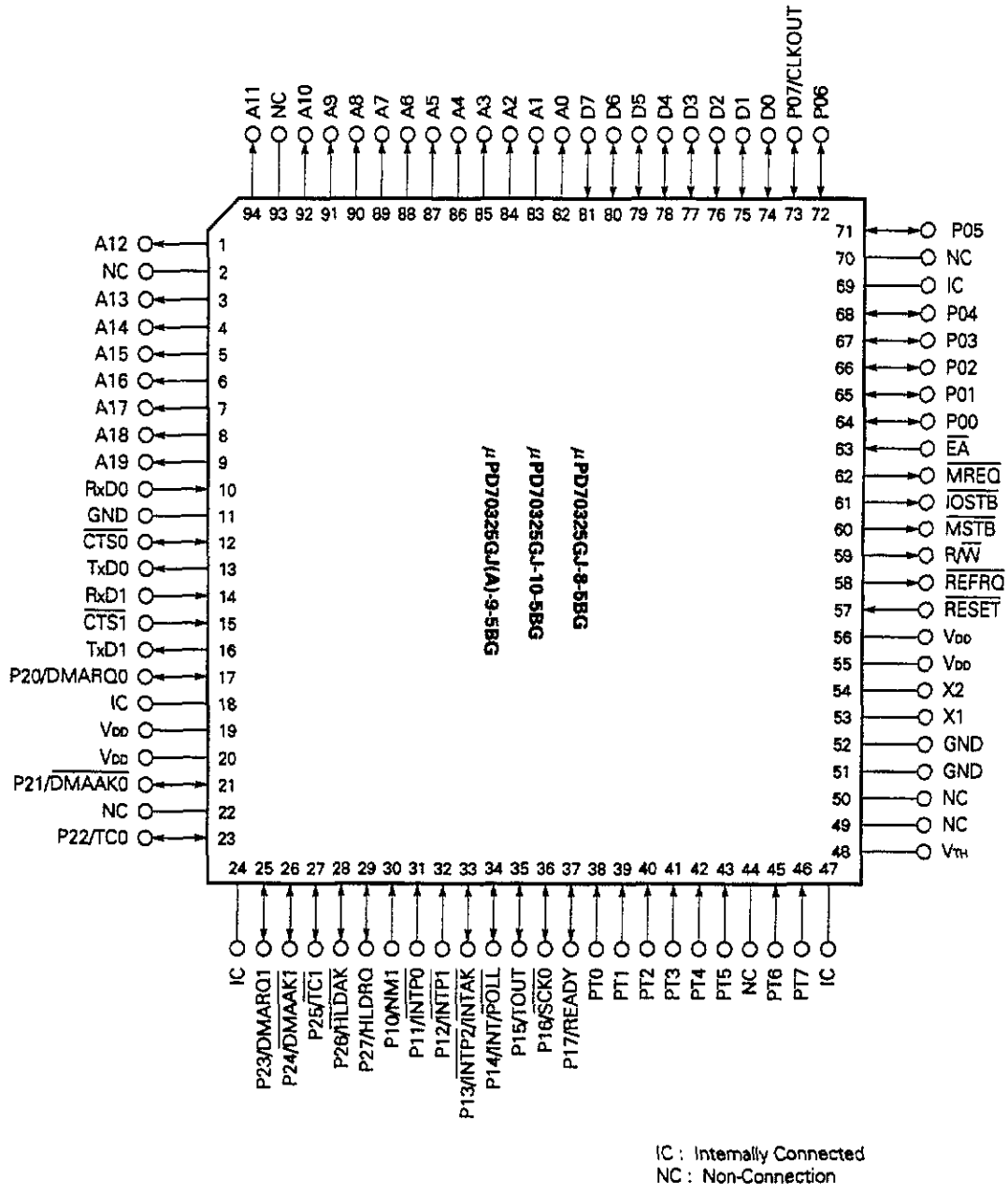


IC : Internally Connected

Cautions
1. **Connect each IC pin to V_{DD} individually via a resistor (3 to 10 kΩ), except for pin 9, which should be connected to GND via a resistor (3 to 10 kΩ).**
2. **Connect the $\overline{EA}$ pin to GND via a resistor (3 to 10 kΩ).**

(2) 94-pin plastic QFP

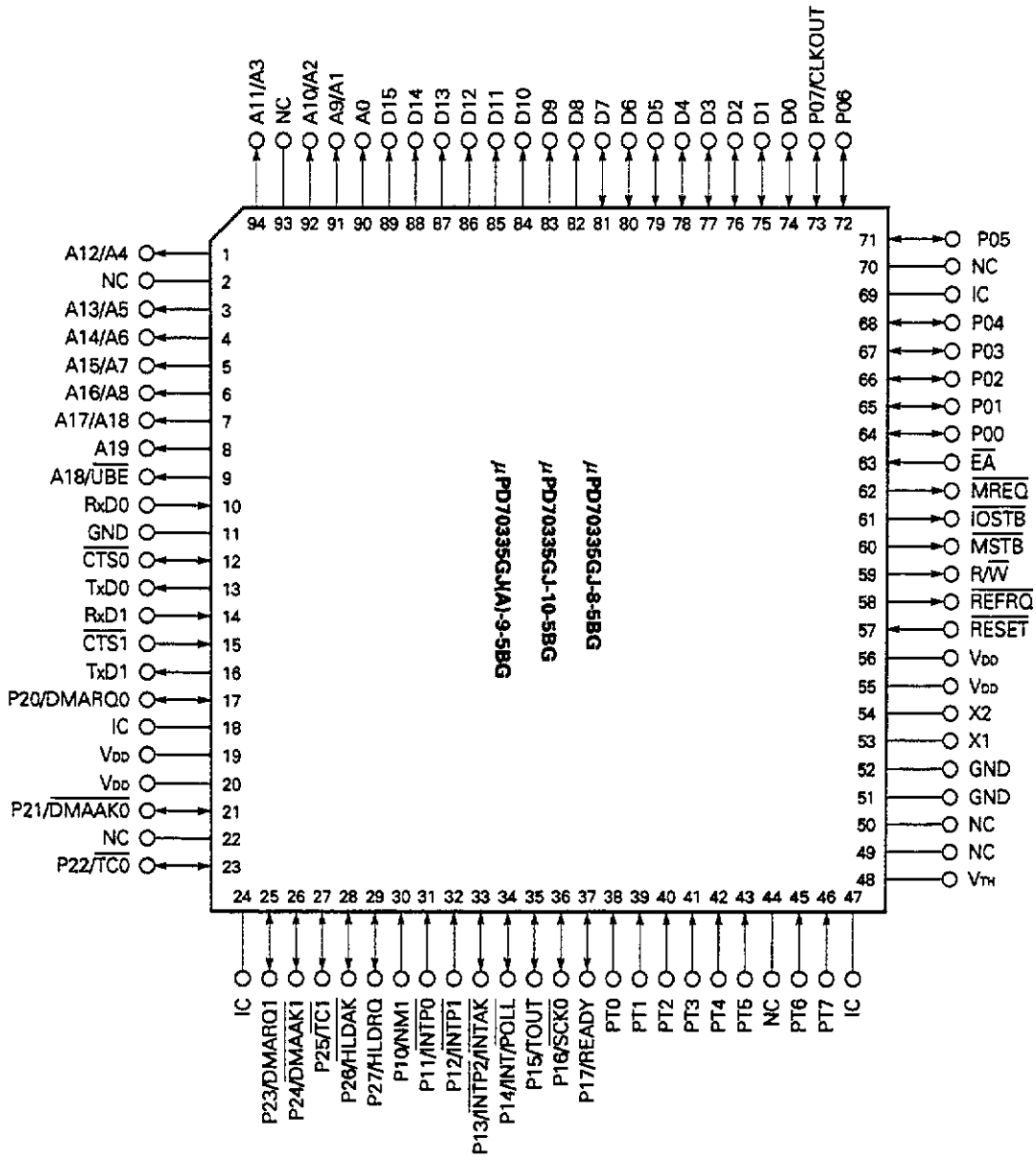
(a) μPD70325



IC : Internally Connected
NC : Non-Connection

Cautions 1. Connect each IC pin to VDD individually via a resistor (3 to 10 kΩ).
2. Connect the $\overline{EA}$ pin to GND via a resistor (3 to 10 kΩ).

(b) μPD70335



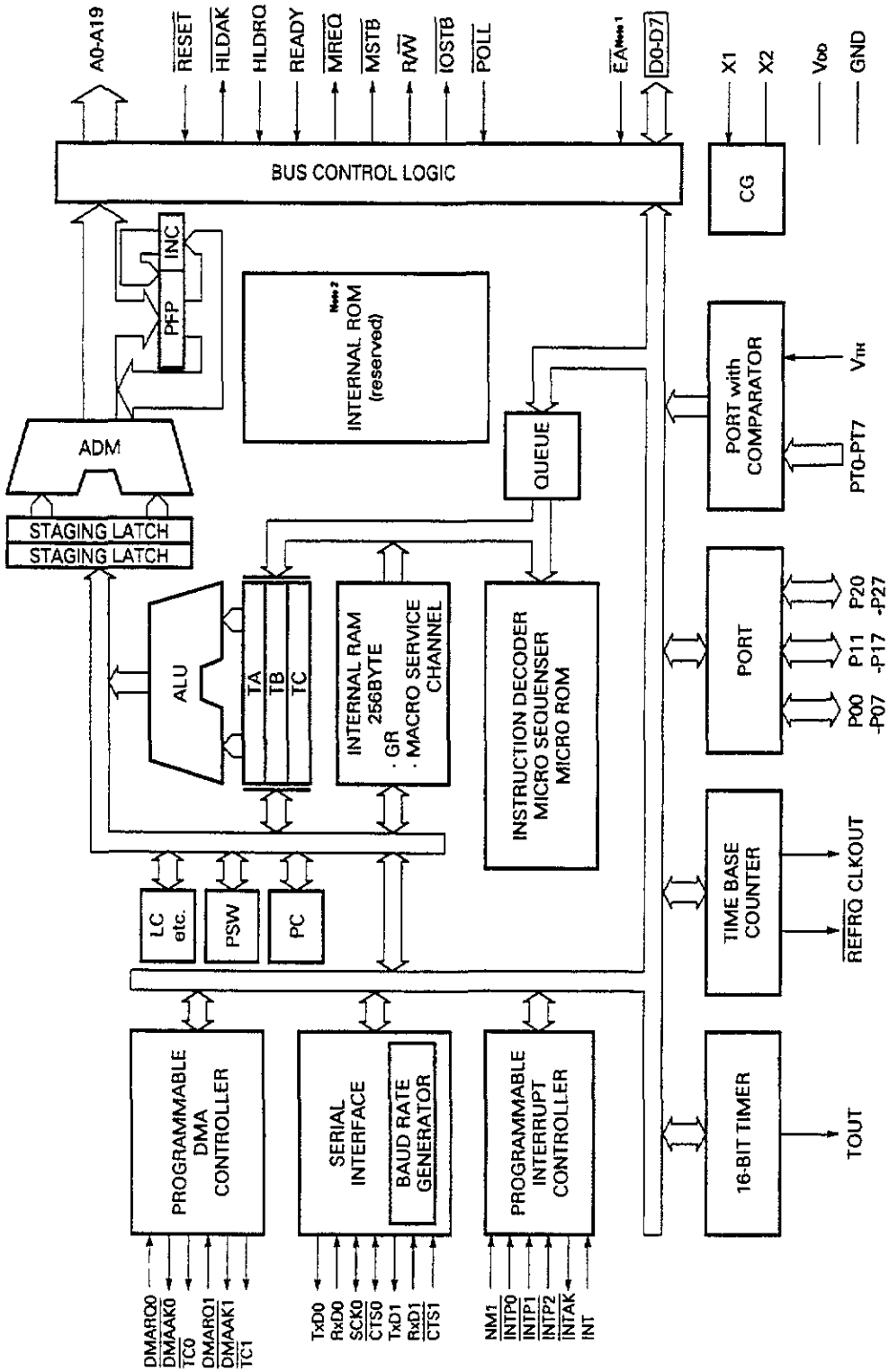
IC : Internally Connected
NC : Non-Connection

Cautions 1. Connect each IC pin to VDD individually via a resistor (3 to 10 kΩ).
2. Connect the $\overline{EA}$ pin to GND via a resistor (3 to 10 kΩ).

$\overline{IOSTB}$	: I/O Strobe	HLDRQ	: Hold Request
$\overline{MREQ}$	: Memory Request	NMI	: Non-Maskable Interrupt Request
P00-P07	: Port 0	$\overline{INTP0}$-$\overline{INTP2}$	: Interrupt From Peripherals
P11-P17	: Port 1	$\overline{INTAK}$	: Interrupt Acknowledge
P20-P27	: Port 2	INT	: Interrupt Request
CLKOUT	: Clock Out	$\overline{POLL}$	: Polling
D0-D15	: Data Bus	TOUT	: Timer Output
A0-A19	: Address Bus	$\overline{SCK0}$	: Serial Clock
RxD0, RxD1	: Receive Data	READY	: Ready
$\overline{CTS0}$, $\overline{CTS1}$	: Clear To Send	PT0-PT7	: Port T
TxD0, TxD1	: Transfer Data	X1, X2	: Crystal
DMARQ0, DMARQ1	: DMA Request	$\overline{RESET}$	: Reset
$\overline{DMAAK0}$, $\overline{DMAAK1}$	: DMA Acknowledge	$\overline{REFRQ}$	: Refresh Request
$\overline{TC0}$, $\overline{TC1}$	: Terminal Count	R/$\overline{W}$	: Read/Write
$\overline{HLDAK}$	: Hold Acknowledge	$\overline{MSTB}$	: Memory Strobe
		$\overline{EA}$	: External Access

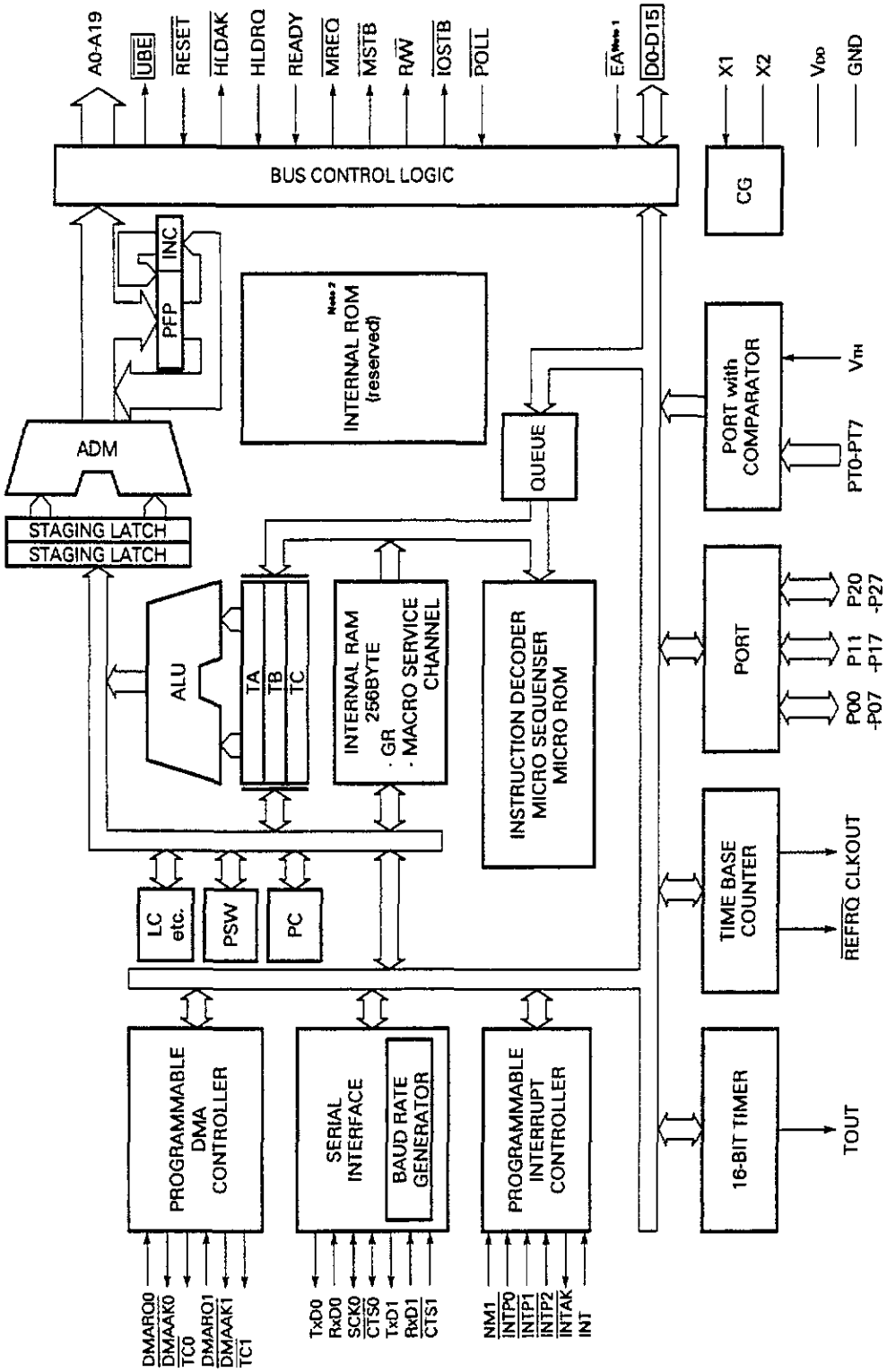
1.5 Internal Block Diagram

1.5.1 μPD70325



Notes 1. Fixed at low level externally.
2. Cannot be used by users.

1.5.2 μPD70335



Notes 1. Fixed at low level externally.

2. Cannot be used by users.

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