CHAPTER 11 SERIAL INTERFACE

11.1 Serial Interface Configuration

The μPD70325 and 70335 each have two on-chip serial interface channels that contain dedicated baud rate generators.

The serial interface is a transfer system using start and stop bits. It provides two operation modes: the asynchronous mode, which uses a start bit for bit synchronization and character synchronization of data; and the I/O interface mode, which transfers data in synchronization with a controlled serial clock, as when using a serial data transfer system such as the μPD7810.

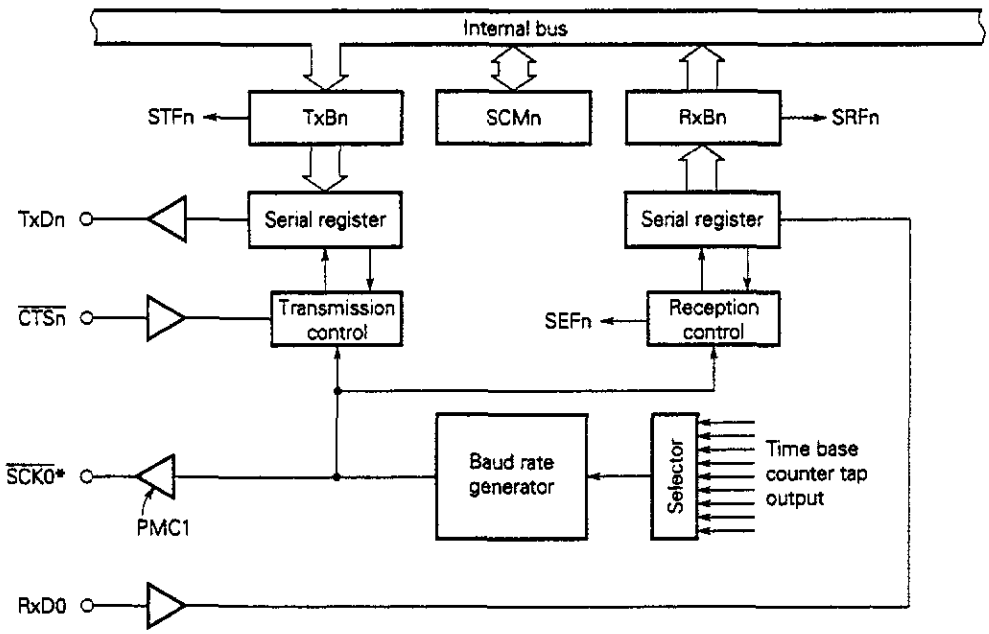
Figures 11-1 (a) and (b) show serial interface block diagrams for when the asynchronous mode and I/O interface mode are set, respectively.

The serial interface consists of a serial data input (RxDn), serial data output (TxDn), serial clock output ($\overline{SCK0}$), and clear to send ($\overline{CTSn}$) pins[Note], a transfer control block, 8-bit serial registers for transmission and reception, a transmit buffer (TxBn), receive buffer (RxBn), and baud rate generator. Because serial registers and buffers are provided for independent transmission and reception, full duplex operation can be performed. In the I/O interface mode, the $\overline{CTSn}$ pin has the receive clock input/output pin function, and full duplex serial operation can also be performed in the I/O interface mode.

Note See section **A.3 Limitations on Send Data Missing by Transmission Disable Operation during Serial Transmission.**

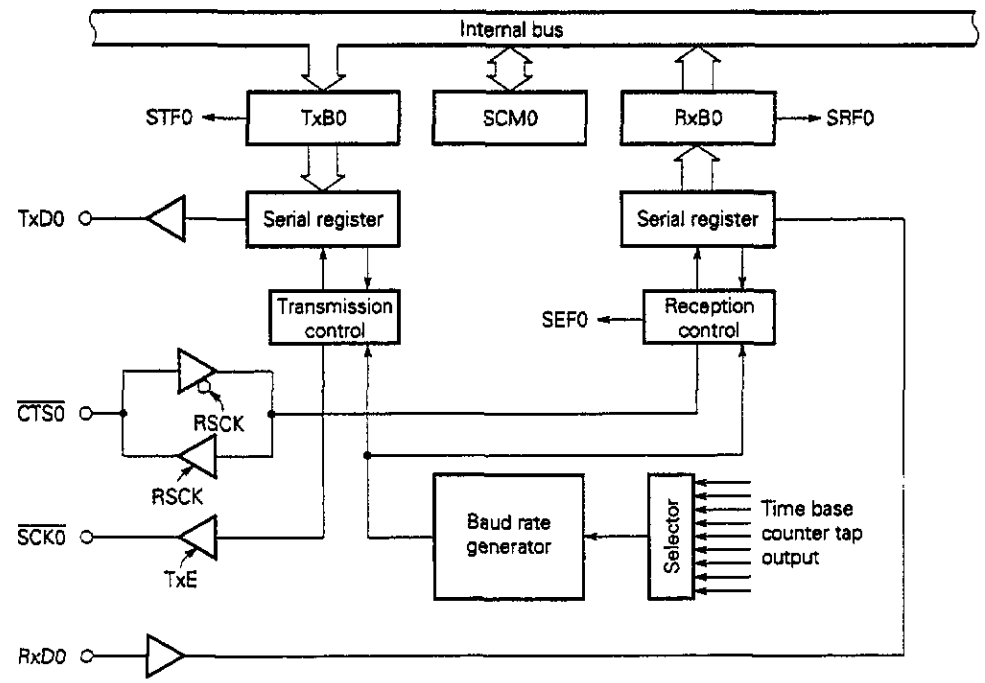
Figure 11-1. Serial Interface Function

(a) When asynchronous mode is set (n = 0 or 1)



* Only channel 0

(b) When I/O interface mode is set (channel 0 only)



11.2 Asynchronous Mode

In the asynchronous mode, the serial mode register (SCMn) can control specification of the character length, number of stop bits, parity enable state, and odd or even parity.

11.2.1 Transmission

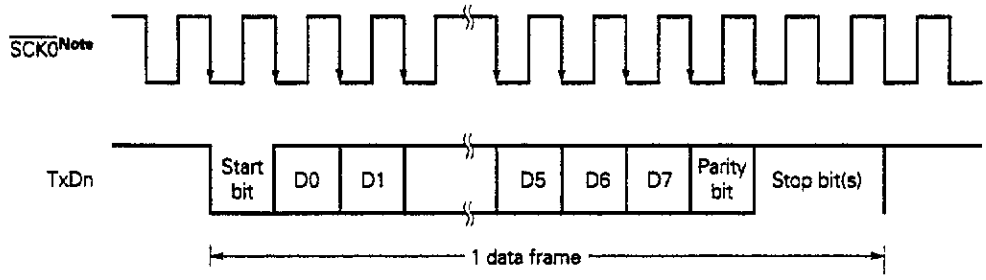
When serial mode register (SCMn) bit 7 (TxRDY) is set to 1 and the $\overline{\text{CTSn}}$ pin is active (0), transmission is enabled **Note**. Transmission can be started in any of the following three ways:

(a) A transmission completion interrupt is generated by enabling transmission when the transmit buffer (TxB) is empty, and the interrupt routine writes send data into the transmit buffer.
(b) If send data is transferred to the transmit buffer when transmission is enabled, the send data is transmitted consecutively after the immediately preceding transmission operation terminates.
(c) If transmission is enabled after send data is prewritten into the transmit buffer in the transmission disable state, the data retained in the transmit buffer is transmitted.

Note Transmission may be enabled by either activating the $\overline{\text{CTSn}}$ pin with TxRDY = 1 or by setting TxRDY to 1 with the $\overline{\text{CTSn}}$ pin activated.

The send data format is shown below. A start bit, character bit, and a parity bit, and one or two stop bits make up one data frame (see **Figure 11-2**). Send data is sent out in synchronization with the transmission clock's falling edge, starting at the least significant bit (LSB) from the TxDn pin. The transmission clock is output from $\overline{\text{SCK0}}$ pin only for channel 0 (not output for channel 1). In this transmission clock, the baud rate of channel 0 is used as a clock number. When transmission is disabled or when there is no data transmitted to the serial register, the TxDn pin becomes the mark state (1).

Figure 11-2. Format of Send Data



Note Only channel 0

Start bit : 1
Character bit : Odd, even, 0, or no parity
Stop bit(s) : One or two

11.2.2 Transmission completion interrupt

A transmission completion interrupt request occurs immediately when the transmit buffer (TxBn) becomes empty.

When $\overline{\text{RESET}}$ is input, the transmit buffer (TxBn) becomes empty. If transmission is enabled at this time, a transmission completion interrupt request occurs. When transmission operation is started and send data in the transmit buffer is transferred to the shift register, the transmit buffer becomes empty and a transmission completion interrupt request occurs.

Consecutive data transmission is enabled without inserting the mark state (1) by writing send data into the transmit buffer each time a transmission completion interrupt request occurs. When transmission is disabled, transfer from the transmit buffer to the shift register is also disabled.

If the transmission enable state is switched to disable during the transmission operation, the data being transmitted is transmitted up to the end of the current frame. However, if new send data is already written into the transmit buffer, transfer from the transmit buffer to the shift register is disabled and the transmit buffer contents are retained. When transmission is again enabled, the transmit buffer contents are transferred to the shift register in synchronization with this timing, and a transmission completion interrupt request occurs concurrently with the start of transmission.

Caution When a transmission completion interrupt is used in a macro service and while a macro service which will set macro service counter (MSC) to 0 is held pending for a long time, another macro service may be processed and the macro service completion interrupt may be acknowledged with the serial register and transmit buffer empty.
In this case, the TxRDY flag of SCM0 and SCM1 must be set from 1 to 0 then 1 (enable → disable → enable) within the macro service completion interrupt service routine. If this operation is not executed, subsequent transmission completion interrupts will not occur and the transmission operation will stop. (For example, this occurs when the interrupt servicing time is long for an interrupt having a higher priority level than the transmission interrupt.) However, all other operations will continue normally.

11.2.3 Reception

When serial mode register (SCM2) bit 6 (RxE) is set to 1, reception is enabled. When reception is disabled (RxE = 0), the reception hardware stands by in the initial state.

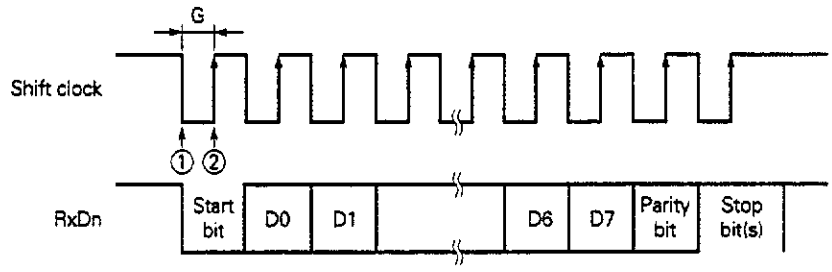
When RxDn pin input is sampled using the input clock to the baud rate generator and the falling edge is detected, reception operation starts and the baud rate generator for reception starts counting. If RxDn pin input is detected to be low with the first timing signal from the baud rate generator for reception, it is recognized as a start bit and subsequent reception operations are performed. If it is detected to be high with the first timing signal, it is not recognized as a start bit and the baud rate generator is initialized and stops operation.

Receive data is sampled in synchronization with the shift clock's rising edge after a start bit is detected (see **Figure 11-3**).

The start bit is detected by the input clock (selected by setting the SCC register) to the baud rate generator. The baud rate is generated by counting the clocks generated by dividing the input clocks by two, as many times as the value (G) set in the BRG register.

In other words, the start bit is detected when G is counted using the input clock's edge to the baud rate generator after the reception pin (RxD) is detected low when sampling the input clock to the baud rate generator. Once the start bit is detected, receive data is read each time 2G is counted by the input clock's edge to the baud rate generator.

Figure 11-3. Receive Data Sampling Timing



① Reception operation starts when the falling edge of the RxD pin is detected when sampling the input clock's edge to the baud rate generator.

② The baud rate generator for reception starts counting.

11.2.4 Reception completion interrupt

Upon reception completion of data having the character length specified in the serial mode register bit 3 (CL), receive data in the shift register is transferred to the receive buffer (RxBn) and a reception completion interrupt request is generated.

During reception, an odd-even parity check is made (when PRTY1 bit[Note] = 1). When a mismatch is found (parity error), when the stop bit is low (framing error), or when the receive buffer is full and the next data is transferred to the receive buffer (overrun error), a reception error flag is set, causing a reception error interrupt request to occur. (See section **11.7**).

Note The PRTY1 bit is serial mode register bit 5.

Caution If the RxE bit is cleared to set the reception disable state during reception, the character being received at the time is not guaranteed.

11.3 I/O Interface Mode

The I/O interface mode is the same as the serial interface mode of the μPD7810, etc. It is useful for external I/O addition or connection of an I/O controller (such as an A/D converter or liquid crystal controller).

In the I/O interface mode, data is transferred starting at the most significant bit (MSB) with the character length fixed to eight bits and with no parity bit.

The I/O interface mode can be used only with channel 0.

11.3.1 Transmission

When serial mode register bit 7 (TxE) is set to 1, transmission is enabled. In the I/O interface mode, the $\overline{SCK0}$ pin is used as a transmit clock output pin.

The transmit clock cannot be externally input.

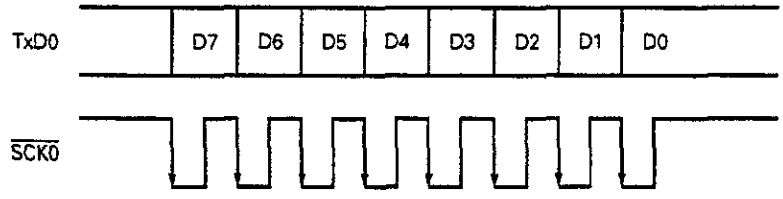
As with the asynchronous mode, transmission operation in the I/O interface mode can be started in any of the following three ways:

(a) A transmission completion interrupt request is generated by enabling transmission when the transmit buffer (TxB0) is empty, and the interrupt service routine writes send data into the transmit buffer.

(b) If send data is transferred to the transmit buffer (TxB0) when transmission is enabled, the send data is transmitted consecutively after the immediately preceding transmission operation terminates.

(c) If transmission is enabled after send data is prewritten into the transmit buffer (TxB0) in the transmission disable state, the data retained in the transmit buffer (TxB0) is transmitted.

The send data format is shown below. The data is transmitted starting at the most significant bit (MSB) with the character length fixed to eight bits.



11.3.2 Transmission completion interrupt

A transmission completion interrupt request occurs immediately when the transmit buffer (TxB0) becomes empty.

When $\overline{RESET}$ is input, the transmit buffer (TxB0) becomes empty. If transmission is enabled at this time, a transmission completion interrupt request occurs. When transmission operation starts and send data in the transmit buffer (TxB0) is transferred to the shift register, the transmit buffer becomes empty and a transmission completion interrupt request occurs.

Caution When a transmission completion interrupt is used in a macro service and while a macro service which will set macro service counter (MSC) to 0 is held pending for a long time, another macro service may be processed and the macro service completion interrupt may be acknowledged with the serial register and transmit buffer empty.
In this case, the TxRDY flag of SCM0 and SCM1 must be set from 1 to 0 then 1 (enable → disable → enable) within the macro service completion interrupt service routine. If this operation is not executed, subsequent transmission completion interrupts will not occur and the transmission operation will stop. (For example, this occurs when the interrupt servicing time is long for an interrupt having a higher priority level than the transmission interrupt.) However, all other operations will continue normally.

11.3.3 Reception

When serial mode register (SCM0) bit 6 (RxE) is set to 1, reception is enabled. Receive data is input to the serial register on the reception clock's rising edge. When the serial register receives 8-bit data, the data is transferred from the serial register to the receive buffer (RxB0) and a reception completion interrupt request is generated.

During I/O interface mode, the reception clock can be selected as either an external reception clock or an internal reception clock by setting the serial mode register (SCM0) bit 2 (RSCK).

When using an internal reception clock, the operation is started by writing a value of 1 into the SCM0 TSK bit. This means that the macro service function cannot be used.

During I/O interface mode, the $\overline{\text{CTS0}}$ pin functions as a reception clock input/output pin.

Caution If the RxE bit is cleared to set the reception disable state during reception, the character being received at the time is not guaranteed.

11.3.4 Reception error interrupt

During reception, if the receive buffer (RxB0) becomes full and the next data is transferred to the receive buffer (overrun error), a reception error flag is set, causing a reception error interrupt request to occur.

11.3.5 Serial register clear

To clear the serial register, perform either of the following operations.

- Write into the SCC0 register
- Change the SCM0 register's MD0 bit
  (I/O interface mode → asynchronous mode → I/O interface mode)

11.4 Starting Transmission without Using Interrupts

Transmission can be started without using interrupts in the following two ways.

(1) If the transmission enable state is set while the transmit buffer (TxB) is empty, the interrupt control register (STICn) bit 7 (STFn) will be set to 1, and should be cleared to 0 once. Next, the send data is written into the transmit buffer, and then the STICn bit is polled to start transmission.

(2) After the first byte of data is written into the transmit buffer (TxB) during the transmission disable state, setting the trasmission enable state causes the data retained in the transmit buffer to be downloaded to the serial register, from where the data is output.

Remark The STICn register's bit 7 (STFn) is not cleared to 0 until a transmission completion interrupt is acknowledged. Accordingly, when not using interrupts, use software to clear the STFn flag to 0 when writing data to the transmit buffer.

11.5 Serial Mode Registers (SCM0 and SCM1)

The serial mode registers (SCMn, n = 0 or 1) are 8-bit registers that specify the serial interface transfer mode. The SCM0 register can be set for channel 0 and the SCM1 register for channel 1. The meanings of SCMn bits 2 to 7 vary depending on how bits 1 and 0 (MD1 and MD0) are set.

7	6	5	4	3	2	1	0
						MD 1	MD 0

MD1, MD0 = 0, 1 (asynchronous mode)

	7	6	5	4	3	2	1	0
SCM0/SCM1	TxRDY	RxE	PRTY 1	PRTY 0	CL	SL	0	1

MD1, MD0 = 0, 0 (I/O interface mode)

	7	6	5	4	3	2	1	0
SCM0	TxE	RxE	0	0	TSK	RSCK	0	0

The MD1 and MD0 bits are serial interface transfer mode specification bits. The asynchronous mode is selected by setting MD1 = 0 and MD0 = 1. The I/O interface mode is selected by setting MD1 = 0 and MD0 = 0. However, the I/O interface mode can be set only in SCM0.

The registers can be written/read by making an 8-bit or 1-bit memory access.

When $\overline{\text{RESET}}$ is input, the register contents are reset to 00H.

During serial transmission, transfer of send data from the transmit buffer (TxB) to the serial register causes an interrupt request flag (STFn) to be set, after which data is sent to the TxD pin one bit at a time.

This means that if the serial mode register (SCMn) is used during serial transmission and immediately after STFn has been set, subsequent transmission operations cannot be performed normally.

Therefore, be sure to allow sufficient time for the transmission operation after data is set into the serial mode register (SCMn).

(1) When asynchronous mode is set

RxE : Reception enable control bit

When RxE is set to 0 (reception disable) during the reception operation, reception processing is stopped and no reception completion interrupt occurs.

SL : Bit specifying the number of stop bits

When the SL bit is reset to 0, one stop bit is specified; when the bit is set to 1, two stop bits are specified.

CL : Character length specification bit

When the CL bit is reset to 0, the character length is set to seven bits; when the bit is set to 1, the character length is set to eight bits.

PRTY0 and PRTY1 : Parity addition specification bits

No parity, odd parity, even parity or 0 parity is specified by setting the PRTY0 and PRTY1 bits. When 0 parity is specified, the parity bit is set to 0 during transmission and is ignored during reception.

TxRDY : Transmission enable state control bit

When the $\overline{CTSn}$ pin is low and TxRDY is set to 1, transmission is enabled.

Figure 11-4. SCM0 and SCM1 (when asynchronous mode is set)

7	6	5	4	3	2	1	0	When reset	R/W
TxRDY	RxE	PRTY1	PRTY0	CL	SL	0	1	00H	R/W

Stop bit length specification

0	One stop bit
1	Two stop bits

Character length specification

0	Seven bits
1	Eight bits

Parity addition specification

PRTY 1	PRTY 0	Parity specification
0	0	No parity
0	1	0 parity[Note]
1	0	Odd parity
1	1	Even parity

Note When 0 parity is specified, the parity bit is set to 0 during transmission and is ignored during reception.

Reception enable control

0	Reception disable
1	Reception enable

Transmission enable control

0	Transmission disable
1	Transmission enable when $\overline{CTSn}$ pin is low

(2) When I/O interface mode is set

RSCK : Serial reception clock source specification bit

When the RSCK bit is reset to 0, the external reception clock is selected for the reception operation; when the bit is set to 1, the internal reception clock is selected for the reception operation. The $\overline{CTS0}$ pin is used as the reception clock input/output pin.

TSK : Reception clock output trigger bit

This bit is valid only when the RSCK bit is set to 1. When 1 is written into the TSK bit, eight reception shift clocks are output from the $\overline{CTS0}$ pin. When serial clock is output, the TSK bit is automatically reset to 0.

RxE : Reception enable control bit

When RxE is set to 1, reception is enabled; when the bit is reset to 0, reception is disabled. If the bit is reset to 0 (reception disable) during the reception operation, reception processing is stopped and no reception completion interrupt request occurs.

TxE : Transmission enable control bit

When the TxE bit is set to 1, transmission is enabled, when the bit is reset to 0, transmission is disabled. If transfer data is written into the transmit buffer when transmission is enabled (TxE = 1), the corresponding serial transmission is started after the transmission being performed or immediately if a transmission is not being performed.

If send data is written into the transmit buffer when transmission is disabled (TxE = 0), serial transmission is not performed and the data in the transmit buffer is retained. Subsequently, transmission processing of the send data held in the transmit buffer is started at the same time as transmission is enabled.

Although the TxE bit is reset to 0 (transmission disable) during the transmission operation, the transmission operation is performed to the end. However, if the next send data is already stored in the transmit buffer when transmission is disabled by resetting TxE to 0, the next send data transmission is held pending and the data is retained in the transmit buffer.

Figure 11-5. SCM0 (when I/O interface mode is set)

7	6	5	4	3	2	1	0	When reset	R/W
TxE	RxE	0	0	TSK	RSCK	0	0	00H	R/W

Reception clock specification

0	External reception clock ($\overline{CTS0}$ pin input mode)
1	Internal reception clock ($\overline{CTS0}$ pin output mode)

Serial interface control

0	-
1	When "1" is written into TSK, eight shift clocks are output

Reception enable control

0	Reception disable
1	Reception enable

Transmission enable control

0	Transmission disable
1	Transmission enable

11.6 Baud Rate Generators

The baud rate generators are 8-bit timers dedicated to the serial interface that generates shift clocks for transmission and reception. Transmission and reception baud rate generators are provided for each channel. The transmission baud rate is the same as the reception baud rate. The baud rate is determined by writing a value to the baud rate generator register (BRGn). However, the maximum baud rate is 750 kbps. Data transfer at more than 750 kbps is enabled by inserting idle time of one shift clock or more between data units.

The input clock to the baud rate generator is specified by selecting a time base counter output tap (see section **10.1**) in serial control register (SCCn) bits PRS3 to PRS0. The baud rate generator output signal is used for the serial interface shift clock. The relationship between the baud rate and parameters is shown below.

$$B \cdot G = 10^6 \times \frac{f_{CLK}}{2^{n+1}}$$

These parameters are defined as follows.

B : Transfer baud rate (bps)
B=110, 150, ·····, 9600, 19200, ·····

G : Value set in baud rate generator register (BRGn) ($2 \leq G \leq 255$)

n : Input clock specification number to baud rate generator specified in serial control register ($0 \leq n \leq 8$)

CLK : System clock frequency (MHz)

The two modes are described as follows.

- When in I/O interface mode (clock synchronization)
  No baud rate error is allowed. The data timing is determined by the setup and hold times corresponding to the transmission and reception clock's rising edge.
- *During asynchronous mode (asynchronously)*
  The baud rate is defined as $(1/G) \times 10^6 \times f_{CLK}/2^{n+1}$ and the baud rate error depends on the f_{CLK} value. When the setup value G is small, the effect of f_{CLK}'s frequency deviation becomes greater. Therefore, the baud rate's error tolerance is reduced as the setup value G becomes smaller.

Table 11-1 lists the baud rate generator setup values for each standard baud rate when an external 16-MHz crystal is used (when $f_{CLK} = f \times 12$).

Table 11-1. Baud Rate Generator Setup Values (for reference)

When f_{CLK} = 8 MHz

Baud rate	n	BRGn register setup value G	Error (%)
110	8	142	0.03
150	7	208	0.16
300	6	208	0.16
600	5	208	0.16
1200	4	208	0.16
2400	3	208	0.16
4800	2	208	0.16
9600	1	208	0.16
19200	0	208	0.16
38400	0	104	0.16

n: Specification number of input clock to baud rate generator

The baud rate error is calculated as follows.

$$\sqrt{\left\{\frac{\left(\begin{array}{l}\text{Baud rate calculated}\\ \text{based on parameters}\end{array}\right)-\left(\begin{array}{l}\text{Requested baud}\\ \text{rate value}\end{array}\right)}{\text{Baud rate value for requested value.}}\right\}^2} \times 100\ (\%)$$

The baud rate error values listed in Table 11-1 are errors corresponding to the requested values for parameter-based settings.

11.6.1 Serial control registers (SCC0 and SCC1)

The serial control registers (SCC0 and SCC1) are serial interface transfer rate control registers.

The registers can be written/read by making an 8-bit or 1-bit memory access.

When $\overline{\text{RESET}}$ is input, the register contents are initialized to 00H.

Time base counter output tap input to the baud rate generator is specified by setting bits PRS3 to PRS0.

Figure 11-6. SCC0 and SCC1

7	6	5	4	3	2	1	0	When reset	R/W
0	0	0	0	PRS 3	PRS 2	PRS 1	PRS 0	00H	R/W

n	PRS 3	PRS 2	PRS 1	PRS 0	Input clock to baud rate generator
0	0	0	0	0	$f_{CLK}/2$
1	0	0	0	1	$f_{CLK}/4$
2	0	0	1	0	$f_{CLK}/8$
3	0	0	1	1	$f_{CLK}/16$
4	0	1	0	0	$f_{CLK}/32$
5	0	1	0	1	$f_{CLK}/64$
6	0	1	1	0	$f_{CLK}/128$
7	0	1	1	1	$f_{CLK}/256$
8	1	0	0	0	$f_{CLK}/512$

f_{CLK}: System clock frequency
n : Specification number of input clock to baud rate generator

11.7 Serial Error and Transmission/Reception State Detection

The following three types of serial interface reception errors can be detected.

(a) Parity error (in asynchronous mode)
The parity operation result does not match the reception parity.
(b) Framing error (in asynchronous mode)
Stop bit is not detected.
(c) Overrun error (in asynchronous or I/O interface mode)
Before the preceding receive data is received from RxB, the next reception is complete.

The following two types of transmission/reception buffer state can be detected.

(a) Transmission buffer empty state
(b) Reception buffer full state

11.7.1 Serial status registers (SCS0 and SCS1)

The serial status registers are 8-bit registers that indicate a reception error status, reception pin status, and transmission/reception buffer data stored status. These registers are provided for both channel 0 and channel 1.

These registers can be only read by making an 8-bit memory access.

The error flags are updated when the next data reception terminates. The previous flag contents are retained until then.

When $\overline{\text{RESET}}$ is input, the SCSn contents are initialized to 60H.

ERPn : Parity error flag

When transmission parity does not match reception parity, the ERP flag is set to 1. If they match at the next data reception, the flag is reset to 0.

ERFn : Framing error flag

When a stop bit is not detected, the ERF flag is set to 1. If a stop bit is detected at the next data reception, the flag is reset to 0.

EROn : Overrun error flag

When the next reception is completed before the preceding receive data is received from the receive buffer (RxB), the ERO flag is set to 1. When data reception terminates after receive data is read from the receive buffer (RxB), the flag is reset to 0.

TxBEn : Transmission buffer empty flag

Flag that indicates the transmission buffer is empty.

It is set (1) when the transmission data in the transmission buffer is transferred to the shift register by a transmission operation and the transmission buffer is empty, or when a value of the baud rate generator register (BRGn) or the serial control register (SCCn) is updated. It is reset (0) when transmission data is written in the transmission buffer.

RxBFn : Reception buffer full flag

Flag that indicates that reception data is stored in the reception buffer.

It is set (1) regardless of the reception error status when reception data is transferred from the shift register to the reception buffer by reception operation. It is reset (0) when reception data is read from the reception buffer or when a value of the baud rate generator register (BRGn) or the serial control register (SCCn) is updated.

ASn : All sent flag

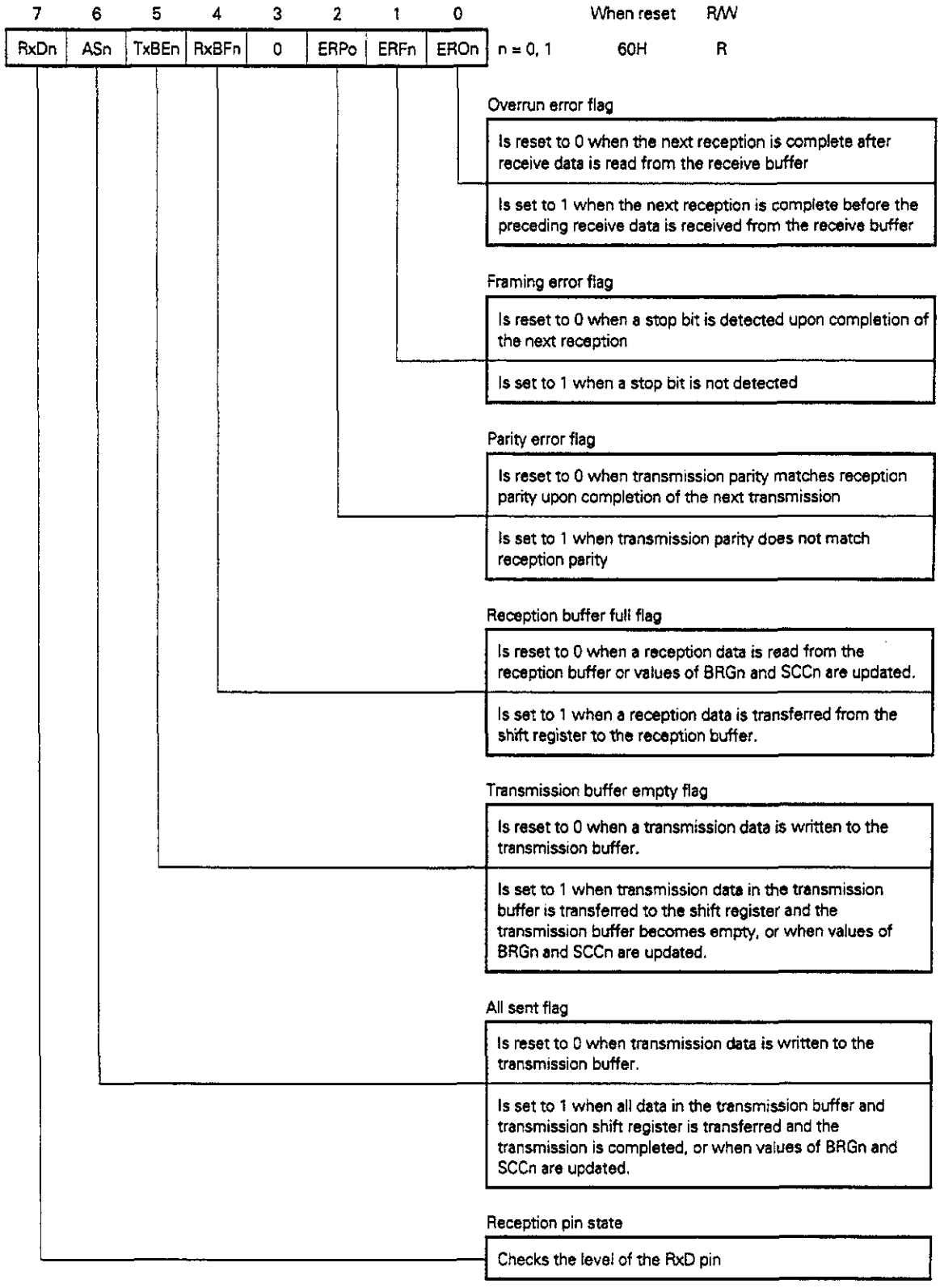
Flag that indicates the transmission buffer and transmission shift register are empty and there is no data in both of them.

It is set (1) when all data in the transmission buffer and transmission shift register is transferred by transmission operation and the transmission is completed, or when a value of the baud rate generator register (BRGn) or the serial control register (SCCn) is updated. It is reset (0) when a transmission data is written in the transmission buffer.

RxDn : Bit for checking the RxD pin for reception state

The RxD pin level is set in this bit.

Figure 11-7. SCS0 and SCS1



11.8 Break State Detection Function

The μPD70325 and 70335 can detect the line break state by software (only in the asynchronous mode). The break state detection procedure is described below.

(1) Reception error interrupt caused by the first framing error

The reception error handling routine checks receive data to ensure that it is 00H. At the same time, the routine checks the reception error flag for framing errors.

(2) Reception error interrupt caused by the second framing error

During the break state, a framing error occurs again.

The line's break state can be determined by the fact that the receive data is again 00H and consecutive 00H data is received with a framing error, and by directly checking the pin state in serial error register (SCEn) bit 7 (RxDn).

11.9 Serial Interface Interrupt Requests

Three types of interrupt requests that occur from the serial interface for both channels (0 and 1) are transmission completion, reception completion, and reception error interrupt requests.

11.9.1 Interrupt request control registers (SEICn, SRICn, and STICn: n = 0 or 1)

The interrupt request control registers are 8-bit registers that control reception error interrupt requests (SEFn), reception completion interrupt requests (SRFn), and transmission completion interrupt requests (STFn); all of which occur from the serial interface.

The three interrupt request control registers make up one group and the priority level can be specified as the serial interface interrupt request group. The priority levels within the group are fixed as follows.

SEFn > SRFn > STFn

When a reception error occurs, a reception error interrupt request is acknowledged preferentially because it has a higher priority level than a reception completion interrupt. When reception error interrupt servicing terminates, the reception completion interrupt is acknowledged.

Figure 11-8. SEICn, SRICn, and STICn (n = 0 or 1)

	7	6	5	4	3	2	1	0
SEIC0/SEIC1	SEFn	SEMKn	MS/$\overline{INT}$	ENCS	0	PR2	PR1	PR0
SRIC0/SRIC1	SRFn	SRMKn	MS/$\overline{INT}$	ENCS	0	1	1	1
STIC0/STIC1	STFn	STMKn	MS/$\overline{INT}$	ENCS	0	1	1	1

Caution Bits 2 to 0 of SRICn and STICn are fixed to 1. The SRICn and STICn interrupt request priority levels conform to the settings for SEICn bits PR2 to PR0.

The SEF, SRFn, and STFn bits are interrupt request flags. When a reception error occurs or when reception or transmission is completed, the SEFn, SRFn, or STFn bit is set to 1. It is reset to 0 by the software or when the corresponding interrupt request is acknowledged.

See section **4.8 Interrupt Request Control Register** for descriptions of the other bits.

The registers can be written/read by making an 8-bit or 1-bit memory access, in which case one wait state is inserted.

When $\overline{RESET}$ is input, the contents of SEICn, SRICn, and STICn are initialized to 47H.

11.9.2 Macro service control registers (SRMSn and STMSn: n = 0 or 1)

The SRMSn register is an 8-bit register that specifies the macro service servicing mode and the channel used when serial interface reception is complete. The STMSn register is an 8-bit register that specifies the macro service servicing mode and the channel used when serial interface transmission is complete. The SRMS0 and STMS0 registers correspond to serial interface channel 0 and the SRMS1 and STMS1 registers correspond to serial interface channel 1.

The registers can be written/read by making an 8-bit or 1-bit memory access, in which case one wait state is inserted.

See section **4.5.4 Macro service control register** for descriptions of the macro service control register bits.

Figure 11-9. SRMSn and STMSn (n = 0 or 1)

7	6	5	4	3	2	1	0
MSM2	MSM1	MSM0	DIR	0	CH2	CH1	CH0