CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function Lists

2.1.1 μPD70325

(1) Ports

Pin name	I/O	Shared by	Function
P00-P06	I/O	–	8-bit I/O port for which the input or output mode can be specified bit-wise
P07		CLKOUT	
P10	I	NMI	Cannot be used as a general purpose port (Nonmaskable interrupt request input)
P11		$\overline{\text{INTP0}}$	Cannot be used as a general purpose port (External interrupt request input)
P12		$\overline{\text{INTP1}}$	
P13		$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$	
P14	I/O	$\overline{\text{POLL}}$/INT	I/O port for which the input or output mode can be specified bit-wise
P15		TOUT	
P16		$\overline{\text{SCK0}}$	
P17		READY	
P20	I/O	DMARQ0	8-bit I/O port for which the input or output mode can be specified bit-wise
P21		$\overline{\text{DMAAK0}}$	
P22		$\overline{\text{TC0}}$	
P23		DMARQ1	
P24		$\overline{\text{DMAAK1}}$	
P25		$\overline{\text{TC1}}$	
P26		$\overline{\text{HLDAK}}$	
P27		HLDRQ	
PT0-PT7	I	–	Input port with an 8-bit comparator

Remark After reset is released, the port pins become input port pins. To use P13/$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$ as an $\overline{\text{INTAK}}$ pin, be sure to connect a pull-up resistor to this pin to avoid external interrupt controller malfunction after reset is released.

(2) Non-port pins

Pin name	I/O	Function	Shared by
$\overline{IOSTB}$	O	I/O read or I/O write strobe output	–
$\overline{MREQ}$		Output indicating that memory bus cycle has started	
CLKOUT		System clock output	P07
D0-D7	I/O	8-bit data bus	–
A0-A19	O	20-bit address output	
RxD0	I	Serial data input	
RxD1			
$\overline{CTS0}$	I/O	Asynchronous mode: CTS input I/O interface mode: reception clock I/O	
$\overline{CTS1}$	I	CTS input	
TxD0	O	Serial data output	
TxD1			
DMARQ0	I	DMA request input (CH0)	P20
DMARQ1		DMA request input (CH1)	P23
$\overline{DMAAK0}$	O	DMA acknowledge output (CH0)	P21
$\overline{DMAAK1}$		DMA acknowledge output (CH1)	P24
$\overline{TC0}$		DMA termination output (CH0)	P22
$\overline{TC1}$		DMA termination output (CH1)	P25
$\overline{HLDAK}$		Hold acknowledge output	P26
HLDRQ	I	Hold request input	P27
NMI		Nonmaskable interrupt request input	P10
$\overline{INTP0}$		External interrupt request input	P11
$\overline{INTP1}$			P12
$\overline{INTP2}$			P13/$\overline{INTAK}$
$\overline{INTAK}$	O	INT acknowledge signal output	P13/$\overline{INTP2}$
$\overline{POLL}$	I	$\overline{POLL}$ input	P14/INT
INT		External interrupt request input	P14/$\overline{POLL}$
TOUT	O	Timer output	P15
$\overline{SCK0}$		Serial clock output	P16
READY	I	Ready input	P17
X1	–	Crystal or ceramic resonator connection pin for system clock oscillation. (External clock can be input to the X1 pin, and inverted clock to the X2 pin.)	–
X2			
$\overline{RESET}$	I	Reset signal input	

Pin name	I/O	Function	Shared by
REFRQ	O	DRAM refresh pulse output	–
R/$\overline{W}$		Read or write cycle identification signal output	
$\overline{MSTB}$		Memory read or memory write strobe output	
V_{TH}	I	Comparator reference voltage input	
V_{DD}	–	Positive power supply pin	
GND		GND pin	
IC		Internally connected (Fix V_{DD} via a resistor)	
$\overline{EA}$		External memory access (Connect to GND via a resistor)	

2.1.2 μPD70335

(1) Ports

Pin name	I/O	Shared by	Function
P00-P06	I/O	–	8-bit I/O port for which the input or output mode can be specified bit-wise
P07		CLKOUT	
P10	I	NMI	Cannot be used as a general purpose port (Nonmaskable interrupt request input)
P11		$\overline{\text{INTP0}}$	Cannot be used as a general purpose port (External interrupt request input)
P12		$\overline{\text{INTP1}}$	
P13		$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$	
P14	I/O	$\overline{\text{POLL}}$/INT	I/O port for which the input or output mode can be specified bit-wise
P15		TOUT	
P16		$\overline{\text{SCK0}}$	
P17		READY	
P20	I/O	DMARQ0	8-bit I/O port for which the input or output mode can be specified bit-wise
P21		$\overline{\text{DMAAK0}}$	
P22		$\overline{\text{TC0}}$	
P23		DMARQ1	
P24		$\overline{\text{DMAAK1}}$	
P25		$\overline{\text{TC1}}$	
P26		$\overline{\text{HLDAK}}$	
P27		HLDRQ	
PT0-PT7	I	–	Input port with an 8-bit comparator

Remark After reset is released, the port pins become input port pins. To use P13/$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$ as an $\overline{\text{INTAK}}$ pin, be sure to connect a pull-up resistor to this pin to avoid external interrupt controller malfunction after reset is released.

(2) Non-port pins

Pin name	I/O	Function	Shared by
$\overline{IOSTB}$	O	I/O read or I/O write strobe output, and low-order address strobe output	–
$\overline{MREQ}$		Output indicating that memory bus cycle or I/O bus cycle has started, and high-order address strobe output	
CLKOUT		System clock output	P07
D0-D15	I/O	16-bit data bus	–
A0	O	LSB of address outputs selecting the low-order memory bank	
A9/A1-A16/A8, A17/A18, A19		19-bit address output by multiplexer	
$\overline{UBE}$	O	Used for address's bit 18 output and selection of high-order memory bank	A18
RxD0	I	Serial data input	
RxD1			
$\overline{CTS0}$	I/O	Asynchronous mode: CTS input I/O interface mode: reception clock I/O	
$\overline{CTS1}$	I	CTS input	
TxD0	O	Serial data output	
TxD1			
DMARQ0	I	DMA request input (CH0)	P20
DMARQ1		DMA request input (CH1)	P23
$\overline{DMAAK0}$	O	DMA acknowledge output (CH0)	P21
$\overline{DMAAK1}$		DMA acknowledge output (CH1)	P24
$\overline{TC0}$		DMA termination output (CH0)	P22
$\overline{TC1}$		DMA termination output (CH1)	P25
$\overline{HLDAK}$		Hold acknowledge output	P26
HLDRQ	I	Hold request input	P27
NMI		Nonmaskable interrupt request input	P10
$\overline{INTP0}$		External interrupt request input	P11
$\overline{INTP1}$			P12
$\overline{INTP2}$			P13/$\overline{INTAK}$
$\overline{INTAK}$	O	INT acknowledge signal output	P13/$\overline{INTP2}$
$\overline{POLL}$	I	$\overline{POLL}$ input	P14/INT
INT		External interrupt request input	P14/$\overline{POLL}$

Pin name	I/O	Function	Shared by
TOUT	O	Timer output	P15
$\overline{SCK0}$		Serial clock output	P16
READY	I	Ready input	P17
X1	I	Crystal or ceramic resonator connection pin for system clock oscillation. (External clock can be input to the X1 pin, and inverted clock to the X2 pin.)	–
X2	–		
$\overline{RESET}$	I	Reset signal input	
$\overline{REFRQ}$	O	DRAM refresh pulse output	
R/$\overline{W}$		Read or write cycle identification signal output	
$\overline{MSTB}$		Memory read or memory write strobe output, and low-order address strobe output	
V_{TH}	I	Comparator reference voltage input	
V_{DD}	–	Positive power supply pin	
GND		GND pin	
IC		Internally connected (Connect to V_{DD} via a resistor)	
$\overline{EA}$		External memory access (Connect to GND via a resistor)	

2.1.3 Pin state in each mode

Pin \ Operation state		Hold	HALT	STOP	During reset	Other
Port	During output in port mode	Held	Held	Held	Hi-Z	Continued
	During output in control mode	Continued	Continued	Held	Hi-Z	Continued
TxD0, TxD1		Continued	Continued	Held	Hi-Z	Continued
$\overline{CTS0}$		Continued	Continued	Held	Hi-Z	Continued
D0-D15		Hi-Z	Hi-Z	Hi-Z	Hi-Z	Continued
A0-A19, $\overline{UBE}$		Hi-Z	Held[Note]	Held[Note]	Hi-Z	Continued
$\overline{MREQ}$		Hi-Z	High	High	Hi-Z	Continued
$\overline{MSTB}$		Hi-Z	High	High	Hi-Z	Continued
R/$\overline{W}$		Hi-Z	High	High	Hi-Z	Continued
$\overline{REFRQ}$		Hi-Z	Continued	Held	Hi-Z	Continued
$\overline{IOSTB}$		Hi-Z	High	High	Hi-Z	Continued

Continued: Specified operation is continued.
Held: The state just before the mode transition is held.
Hi-Z: High impedance

Note Address data is held, but output address is undefined.

2.2 Description of Pin Functions

The μPD70325 and 70335 include both dedicated control pins and pins that have dual functions as ports. For details of the setup method for pins that have dual functions as ports and for information on the hardware configuration, see **CHAPTER 7 PORT FUNCTIONS**.

2.2.1 P00 to P07 (Port 0) - 3-state input/output

P00 to P07 are 8-bit I/O pins for port 0 (8-bit I/O port with output latch). The P07 pin also serves as CLKOUT output.

The P00 to P06 pins operate only in the port mode. The port or control mode can be selected for the P07 pin by setting the port 0 mode control register (PMC0). (See **Table 2-1**.)

Table 2-1. Operation of Port 0 (n = 0 to 7)

	PMC0n = 1	PMC0n = 0	
		PM0n = 1	PM0n = 0
P00	—	Input port	Output port
P01	—	Input port	Output port
P02	—	Input port	Output port
P03	—	Input port	Output port
P04	—	Input port	Output port
P05	—	Input port	Output port
P06	—	Input port	Output port
P07	CLKOUT output	Input port	Output port

(1) Port mode

The input or output mode can be selected for the P00 to P07 pins bit-wise by setting the port 0 mode register (PM0). However, the P07 pin is set to the port mode by setting a value of 0 for PMC0 register bit 7.

(2) Control mode

When the P07 pin is set to the control mode by setting a value of 1 for the PMC0 register bit 7, the pin serves as a CLKOUT output.

(a) CLKOUT (Clock Out) - output also used for P07

CLKOUT is a system clock (CLK) output pin that supplies various clocks to the CPU and peripheral hardware at the frequency set by the clock generator.

In the hold or standby mode, the pins set as output ports hold the immediately preceding data. When the P07 pin is set to CLKOUT, it continues clock output in the hold or HALT mode and holds the immediately preceding data in the STOP mode.

When $\overline{\text{RESET}}$ is input, the P00 to P07 pins operate as an input port (high impedance output).

2.2.2 P10 to P17 (Port 1) - 3-state I/O

P10 to P17 are 8-bit I/O pins used for both port 1 (8-bit I/O with output latch) and for various control signals.

The port or control mode can be selected for the P10 to P17 pins bit-wise by setting the port 1 mode control register (PMC1). (See **Table 2-2.**) However, the P11 and P12 pins operate only in the port mode and also serve as interrupt request input. The P10 pin serves only as an NMI input.

Table 2-2. Operation of Port 1 (n = 0 to 7)

	PMC1n = 1	PMC1n = 0	
		PM1n = 1	PM1n = 0
P10	—	NMI input	—
P11	—	$\overline{\text{INTP0}}$ input	—
P12	—	$\overline{\text{INTP1}}$ input	—
P13	$\overline{\text{INTAK}}$ output	$\overline{\text{INTP2}}$ input	—
P14	INT input	Input port ($\overline{\text{POLL}}$ input)	Output port
P15	TOUT output	Input port	Output port
P16	$\overline{\text{SCK0}}$ output	Input port	Output port
P17	READY input	Input port	Output port

(1) Port mode

When the P10 to P17 pins are set to the port mode by setting the PMC1 register (PMC1n = 0; n = 0 to 7), the input or output mode can be selected for the pins bit-wise by setting the port 1 mode register (PM1). The P10 to P13 pins can operate only as an input port and can also serve as interrupt request input. When the P14 pin is set to an input port, the pin also serves as a $\overline{\text{POLL}}$ input.

(a) NMI (Non-Maskable Interrupt) - P10 input

NMI is an input pin for nonmaskable interrupt requests; this pin cannot be masked by software. Nonmaskable interrupts are acknowledged by the CPU at any time, and they take precedence over any other interrupt.

NMI input is edge-triggered, with the valid edge specified in the external interrupt mode register (INTM).

The input is sampled in each clock cycle. NMI is acknowledged when the pin level is changed from inactive to active level and continues the active level for a certain period or more. When NMI is acknowledged, *an interrupt of vector number 2 occurs after the instruction being executed terminates.*
The NMI input is also used to release the CPU standby mode.
The NMI input state can be monitored by reading P10.

(b) $\overline{\text{INTP0}}$ to $\overline{\text{INTP2}}$ (Interrupt from Peripheral 0 to 2) - input also used for P11 to P13

These are external interrupt request input pins that can be masked by software.
$\overline{\text{INTPn}}$ (n = 0 to 2) is edge-triggered, with the valid edge specified in the external interrupt mode register (INTM). The input is sampled in each clock cycle. INTPn (n = 0 to 2) is acknowledged when the pin level is changed from inactive to active level and continues the active level for a certain period or more.
The $\overline{\text{INTPn}}$ input is also used to release the HALT mode.

(c) $\overline{\text{POLL}}$ (Poll) - input also used for P14/INT

$\overline{\text{POLL}}$ input is checked by the POLL instruction. If it is low, the next instruction is executed. If it is high, $\overline{\text{POLL}}$ input is checked at every fifth clock cycle until it goes low.
These functions are used to synchronize the CPU program with external device operations.

Caution The $\overline{\text{POLL}}$ pin functions when the input mode (input port, INT input) has been selected for P14.
Otherwise, it is assumed to be low while the POLL instruction is being executed.

(2) Control mode

Pins P13 to P17 can be set to control mode bit-wise by setting the PMC1 register.

(a) $\overline{\text{INTAK}}$ (Interrupt Acknowledge) - output also used for P13/$\overline{\text{INTP2}}$

$\overline{\text{INTAK}}$ is an acknowledge signal output pin for interrupt request input (INT) that can be masked by software.
When the CPU acknowledges the INT signal, the $\overline{\text{INTAK}}$ signal is output low. In synchronization with the signal, the external device sends an interrupt vector to the CPU via the data bus (D0 to D15).
$\overline{\text{INTAK}}$ is used in tandem with the INT pin to connect to an interrupt controller such as the μPD71059.

(b) INT (Interrupt) - input also used for P14/$\overline{\text{POLL}}$

INT is an interrupt request input pin that can be masked by software.

This request input, which is active high, is sampled in the last clock cycle of an instruction. By receiving the $\overline{\text{INTAK}}$ signal that is output by the CPU, the external device recognizes that the INT interrupt request is acknowledged. *The INT signal must be held high at least until the first $\overline{\text{INTAK}}$ signal is output.*

The INT pin is used in tandem with the $\overline{\text{INTAK}}$ pin to connect to an interrupt controller such as the μPD71059.

The INT input is also used to release the HALT mode.

(c) TOUT (Timer Output) - output also used for P15

TOUT is an output pin from the timer unit (timer 0).

(d) $\overline{\text{SCK0}}$ (Serial Clock 0) - output also used for P16

$\overline{\text{SCK0}}$ is a serial interface (channel 0) transmission clock output pin.

(e) READY (Ready) - input also used for P17

READY is an input pin used to control wait state insertion during external bus cycles (except memory refresh cycles).

The READY pin is level-sensitive, and wait states are inserted while the READY pin is low.

Caution The bus cycle always becomes ready when the pin is set to P17.

The pins set as an output port hold the immediately preceding data in the hold or standby mode. Control signal output pins that have been set to the control mode continue operation when in the hold or HALT mode, and hold the immediately preceding data when in the STOP mode.

When $\overline{\text{RESET}}$ is input, the P00 to P17 pins operate as an input port (high impedance output).

2.2.3 P20 to P27 (Port 2) - 3-state I/O

P20 to P27 are 8-bit I/O pins used for both port 2 (8-bit I/O port with output latch) and for various control signals.

The port or control mode can be selected as the operation mode for P20 to P27 bit-wise by setting the port 2 mode control register (PMC2). (See **Table 2-3.**)

Table 2-3. Operation of Port 2 (n = 0 to 7)

	PMC2n = 1	PMC2n = 0	
		PM2n = 1	PM2n = 0
P20	DMARQ0 input	Input port	Output port
P21	$\overline{\text{DMAAK0}}$ output	Input port	Output port
P22	$\overline{\text{TC0}}$ output	Input port	Output port
P23	DMARQ1 input	Input port	Output port
P24	$\overline{\text{DMAAK1}}$ output	Input port	Output port
P25	$\overline{\text{TC1}}$ output	Input port	Output port
P26	$\overline{\text{HLDAK}}$ output	Input port	Output port
P27	HLDRQ input	Input port	Output port

(1) Port mode

When P20 to P27 are set to the port mode by setting the PMC2 register (PMC2n = 0; n = 0 to 7), the pins can be set bit-wise to input or output port mode by setting the port 2 mode register (PM2).

(2) Control mode

P20 to P27 can be set to control mode bit-wise by setting the PMC2 register (PMC2n = 1; n = 0 to 7).

(a) DMARQ0 and DMARQ1 (DMA Requests 0 and 1) - input also used for P20 and P23

DMARQ0 and DMARQ1 are DMA request input pins from DMA controllers (channels 0 and 1). These signals are active high.

(b) $\overline{\text{DMAAK0}}$ and $\overline{\text{DMAAK1}}$ (DMA Acknowledge 0 and 1) - output also used for P21 and P24

$\overline{\text{DMAAK0}}$ and $\overline{\text{DMAAK1}}$ are DMA acknowledge output pins to DMA controllers (channels 0 and 1). However, the signals are not output during DMA transfer between memories (burst mode or single step mode).

These signals are active low.

(c) $\overline{\text{TC0}}$ and $\overline{\text{TC1}}$ (Terminal Count 0 and 1) - output also used for P22 and P25

$\overline{\text{TC0}}$ and $\overline{\text{TC1}}$ are DMA completion signal output pins to DMA controllers (channels 0 and 1). The signals are output when $\overline{\text{TC0}}$ and $\overline{\text{TC1}}$ in the DMA service channels are set to 0.

These signals are active low.

(d) $\overline{\text{HLDAK}}$ (Hold Acknowledge) - output also used for P26

$\overline{\text{HLDAK}}$ is an acknowledge signal output pin indicating that the μPD70325 or 70335 has acknowledged the hold request signal (HLDRQ) and has set the bus for high impedance.

While the signal is active (low), the address bus, data bus, and control bus are placed into high-impedance.

(e) HLDRQ (Hold Request) - input also used for P27

HLDRQ is a signal input pin for an external device that requests the μPD70325 or 70335 to release the address bus, data bus, and control bus.

The HLDRQ input signal is active high.

The pins set as an output port hold the immediately preceding data in the hold or standby mode. Control signal output pins that have been set to the control mode continue operation when in the hold or HALT mode, and hold the immediately preceding data when in the STOP mode.

When $\overline{\text{RESET}}$ is input, the P20 to P27 pins operate as an input port (high impedance output).

2.2.4 PT0 to PT7 (Port with Comparator 0 to 7) - input

Port T (PT0 to PT7) consists of 8-bit input pins with a comparator, for which the threshold voltage (reference voltage) can be selected from among 16 levels.

2.2.5 V_{TH} (Threshold Voltage) - input

V_{TH} is a reference voltage input pin for port T.

2.2.6 TxD0 and TxD1 (Transmit Data 0 and 1) - output

TxD0 and TxD1 are serial data output pins from the serial interface (channels 0 and 1).

In the asynchronous mode, transmit data is transmitted with one data frame consisting of start, character, parity, and stop bits, starting at the least significant bit (LSB). When transmission is disabled or when the serial register does not contain the transmit data, the TxD0 and TxD1 pins become the mark state (1).

In the I/O interface mode (TxD0 pin only), transmit data is fixed to eight bits and is transmitted starting at the most significant bit (MSB).

The TxD0 and TxD1 pins continue operation in the hold or HALT mode and hold the immediately preceding data in the STOP mode. When $\overline{\text{RESET}}$ is input, the pins become high impedance.

2.2.7 RxD0 and RxD1 (Receive Data 0 and 1) - input

RxD0 and RxD1 are serial data input pins to the serial interface (channels 0 and 1).

In the asynchronous mode, when RxD0 or RxD1 input is detected low in the reception enable state, it is recognized as a start bit and reception operation is performed.

In the I/O interface mode (RxD0 pin only), receive data is input to the serial register in synchronization with the reception clock's rising edge.

2.2.8 $\overline{\text{CTS0}}$ (Clear to Send 0) - I/O

$\overline{\text{CTS0}}$ is a serial interface (channel 0) CTS pin.

In the asynchronous mode, the $\overline{\text{CTS0}}$ pin is an active low input pin that enables transmission (clear to send). In the I/O interface mode, it becomes an I/O pin for the reception clock.

The $\overline{\text{CTS0}}$ pin continues operation in the hold or HALT mode and holds the immediately preceding data in the STOP mode. When $\overline{\text{RESET}}$ is input, $\overline{\text{CTS0}}$ becomes an input pin in the I/O interface mode (high impedance output).

2.2.9 $\overline{\text{CTS1}}$ (Clear to Send 1) - input

$\overline{\text{CTS1}}$ is a serial interface (channel 1) CTS pin.

The $\overline{\text{CTS1}}$ pin is an active-low input pin that enables transmission (clear to send) when in asynchronous mode.

2.2.10 $\overline{\text{RESET}}$ (Reset) - input

$\overline{\text{RESET}}$ is an active-low reset input pin.

$\overline{\text{RESET}}$ input is an asynchronous input. When a signal having a given low level width is input independently of the operation clock, system reset takes precedence over any other operation that is to be performed.

In addition to normal initialization and start, the $\overline{\text{RESET}}$ pin is also used for standby (STOP or HALT) mode release.

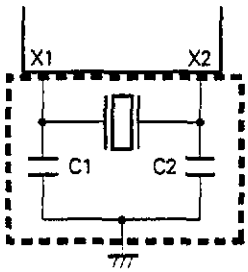
2.2.11 $\overline{\text{EA}}$ (External Access) - input

$\overline{\text{EA}}$ *is an input pin for memory access. Connect this pin to GND via a resistor (3 to 10 kΩ).*

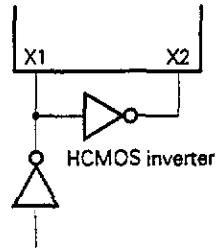
2.2.12 X1 and X2 (Crystal)

X1 and X2 are crystal or ceramic resonator connection pins for system clock generation. An external clock can also be input.

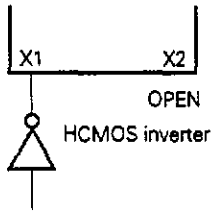
(a) Crystal or ceramic oscillation Note



(b) External clock input



(c) External clock input (X2: Open)



Cautions 1. Place the oscillator as close as possible to X1 and X2.

2. Do not pass any of the signal lines through the area indicated with dotted lines.

Note When considering a match for this device, use a ceramic resonator and external capacitors recommended by NEC Corporation for better device matching.

2.2.13 D0 to D15 (Data Bus 0 to 15) - I/O

D0 to D15 are data bus I/O pins.

In the hold or standby mode or when $\overline{\text{RESET}}$ is input, all of these pins are placed into high impedance.

2.2.14 A0 to A19 (Address Bus 0 to 19) - output

A0 to A19 are 20-bit address bus output pins.

In the standby mode, address data is held but the output address is undefined. In the hold mode or when $\overline{\text{RESET}}$ is input, A0 to A19 are placed into high impedance.

2.2.15 $\overline{\text{MREQ}}$ (Memory Request) - output

$\overline{\text{MREQ}}$ is an active low output pin which indicates that a memory bus cycle has started and that the memory address on the address bus is valid.

In the standby mode, $\overline{\text{MREQ}}$ is fixed high. In the hold mode or when $\overline{\text{RESET}}$ is input, $\overline{\text{MREQ}}$ is placed into high impedance.

2.2.16 $\overline{\text{MSTB}}$ (Memory Strobe) - output

The $\overline{\text{MSTB}}$ pin is an output pin for controlling memory access in combination with the $\overline{\text{MREQ}}$ and R/$\overline{\text{W}}$ signals.

This pin indicates that the data output on the data bus is valid during memory write. $\overline{\text{MSTB}}$ output differs from the $\overline{\text{MREQ}}$ signal only in its fall timing.

In the standby mode, $\overline{\text{MSTB}}$ is fixed high. In the hold mode or when $\overline{\text{RESET}}$ is input, $\overline{\text{MSTB}}$ is placed into high impedance.

2.2.17 R/$\overline{\text{W}}$ (Read/Write Strobe) - output

R/$\overline{\text{W}}$ is a signal output pin for identifying memory read or memory write cycles when a memory bus cycle has started.

For R/$\overline{\text{W}}$, output high indicates a memory read cycle and output low indicates a memory write cycle.

In the standby mode, R/$\overline{\text{W}}$ is fixed high. In the hold mode or when $\overline{\text{RESET}}$ is input, R/$\overline{\text{W}}$ is placed into high impedance.

2.2.18 $\overline{\text{REFRQ}}$ (Refresh Request) - output

$\overline{\text{REFRQ}}$ is a refresh pulse output pin.

$\overline{\text{REFRQ}}$ pin output is controlled by the refresh mode register (RFM) contents. In the HALT mode, the refresh operation is continued. In the STOP mode, the immediately preceding data is held. In the hold mode or when $\overline{\text{RESET}}$ is input, $\overline{\text{REFRQ}}$ is placed into high impedance.

2.2.19 $\overline{\text{IOSTB}}$ (I/O Strobe) - output

$\overline{\text{IOSTB}}$ is an active-low output pin indicating that an I/O bus cycle has started.

When the $\overline{\text{IOSTB}}$ pin is low, it indicates that the I/O address output to the A0 to A15 pins is valid.

In the standby mode, the pin is fixed high. In the hold mode or when $\overline{\text{RESET}}$ is input, $\overline{\text{IOSTB}}$ is placed into high impedance.

2.2.20 V_{DD} (Power Supply)

V_{DD} is a positive power supply pin.

Apply the rated power supply voltage to both V_{DD} pins.

2.2.21 GND (Ground)

GND is a GND potential pin.

Fix all GND pins to the GND potential.

2.2.22 $\overline{\text{UBE}}$ (Upper Byte Enable) - input

$\overline{\text{UBE}}$ is a high-order memory bank selection pin on the μPD70335. It is also used for A18.

This signal becomes active during the following bus cycles.

- Byte access to an odd address, or first byte access to an odd address for word data access
- Word data access to an even address

Access		$\overline{\text{UBE}}$	A0
Word access to even address		0	0
Word access to odd address	First	0	1
	Second	1	0
Byte access to even address		1	0
Byte access to odd address		0	1

The operation described above is also effective in the I/O cycle.

2.3 Pin I/O Circuits

Section **2.3.1** lists the I/O circuit types. Section **2.3.2** shows the circuits for each type.

2.3.1 I/O circuit types

(1) Ports

Pin name	Type	Pin name	Type
P00-P06	5	P20/DMARQ0	5
P07/CLKOUT	5	P21/$\overline{\text{DMAAK0}}$	5
P10/NMI	2	P22/$\overline{\text{TC0}}$	5
P11/$\overline{\text{INTP0}}$	1	P23/DMARQ1	5
P12/$\overline{\text{INTP1}}$	1	P24/$\overline{\text{DMAAK1}}$	5
P13/$\overline{\text{INTP2}}$/$\overline{\text{INTAK}}$	5	P25/$\overline{\text{TC1}}$	5
P14/INT/$\overline{\text{POLL}}$	5	P26/$\overline{\text{HLDAK}}$	5
P15/TOUT	5	P27/HLDRQ	5
P16/$\overline{\text{SCK0}}$	5	PT0-PT7	7
P17/READY	5		

(2) Non-port pins

(a) μPD70325

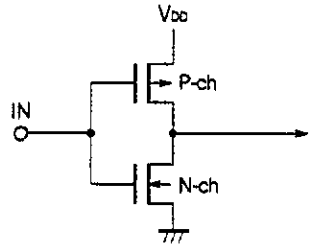
Pin name	Type	Pin name	Type
TxD0	4	$\overline{\text{EA}}$	1
TxD1	4	D0-D7	5
RxD0	1	A0-A19	4
RxD1	1	$\overline{\text{MREQ}}$	4
$\overline{\text{CTS0}}$	5	$\overline{\text{MSTB}}$	4
$\overline{\text{CTS1}}$	1	R/$\overline{\text{W}}$	4
$\overline{\text{REFRQ}}$	4	$\overline{\text{IOSTB}}$	4
$\overline{\text{RESET}}$	2		

(b) μPD70335

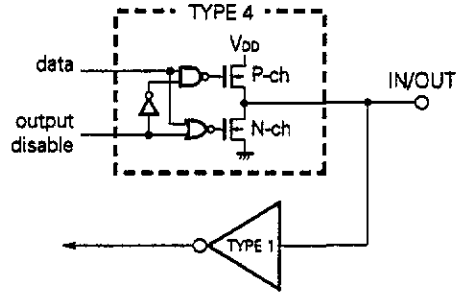
Pin name	Type	Pin name	Type
TxD0	4	A0	4
TxD1	4	A9/A1-A16/A8	4
RxD0	1	A17/A18	4
RxD1	1	A19	4
$\overline{\text{CTS0}}$	5	A18/$\overline{\text{UBE}}$	4
$\overline{\text{CTS1}}$	1	$\overline{\text{MREQ}}$	4
$\overline{\text{REFRQ}}$	4	$\overline{\text{MSTB}}$	4
$\overline{\text{RESET}}$	2	R/$\overline{\text{W}}$	4
$\overline{\text{EA}}$	1	$\overline{\text{IOSTB}}$	4
D0-D15	5		

2.3.2 I/O circuits

TYPE 1

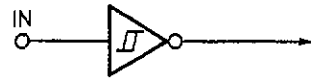


TYPE 5



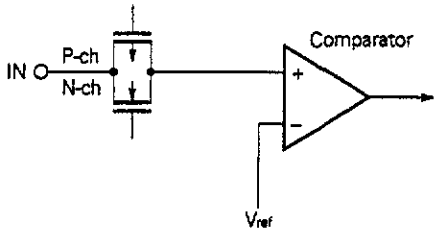
I/O circuit consisting of type-4 push-pull output and type-1 input buffer.

TYPE 2



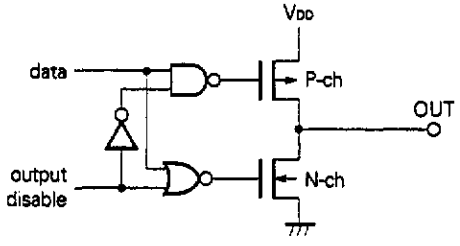
Schmitt trigger input having hysteresis characteristics[Note].

TYPE 7



(Threshold voltage)

TYPE 4



Push-pull output that can be set to high-impedance output (both P-ch and N-ch off).

Note These circuits have been designed for light hysteresis characteristics. However, if the characteristics required for input to these pins are not satisfied, be sure to connect externally to a device that has the required hysteresis characteristics.

2.4 Unused Pin Connections

When connecting to V_{DD} or GND via a resistor, use 3 to 10 kΩ of resistance. Recommended connection methods for unused pins are listed below.

(1) Ports

Pin name	Recommended connection
P00-P06	Input state: Connect each to V_{DD} individually via a resistor.
P07/CLKOUT	Output state: No connection
P10/NMI	Connect to GND via a resistor.
P11/$\overline{INTP0}$	Connect to V_{DD} or GND via a resistor.
P12/$\overline{INTP1}$	
P13/$\overline{INTP2}$/$\overline{INTAK}$	Input state: Connect each to V_{DD} individually via a resistor.
P14/INT/$\overline{POLL}$	Output state: No connection
P15/TOUT	
P16/$\overline{SCK0}$	
P17/READY	
P20/DMARQ0	
P21/$\overline{DMAAK0}$	
P22/$\overline{TC0}$	
P23/DMARQ1	
P24/$\overline{DMAAK1}$	
P25/$\overline{TC1}$	
P26/$\overline{HLDAK}$	
P27/HLDRQ	
PT0-PT7	Connect to GND via a resistor.

Remark *After reset is released, the port pins become input port pins.*

(2) Non-port pins

(a) μPD70325

Pin name	Recommended connection
TxD0	No connection
TxD1	
RxD0	Connect to V_{DD} or GND via a resistor.
RxD1	
$\overline{CTS0}$	Input state: Connect each to V_{DD} individually via a resistor. Output state: No connection
$\overline{CTS1}$	Connect to V_{DD} or GND via a resistor.
$\overline{REFRQ}$	No connection
V_{TH}	Connect to GND via a resistor.
D0-D7	Input state: Connect each to V_{DD} individually via a resistor. Output state: No connection
A0-A19	No connection
$\overline{MREQ}$	
$\overline{MSTB}$	
R/$\overline{W}$	
$\overline{IOSTB}$	

(b) μPD70335

Pin name	Recommended connection
TxD0	No connection
TxD1	
RxD0	Connect to V_{DD} or GND via a resistor.
RxD1	
$\overline{CTS0}$	Input state: Connect each to V_{DD} individually via a resistor. Output state: No connection
$\overline{CTS1}$	Connect to V_{DD} or GND via a resistor.
$\overline{REFRQ}$	No connection
V_{TH}	Connect to GND via a resistor.
D0-D15	Input state: Connect each to V_{DD} individually via a resistor. Output state: No connection
A0	No connection
A9/A1-A16/A8	
A17-A18	
A19	
A18/$\overline{UBE}$	
$\overline{MREQ}$	
$\overline{MSTB}$	
R/$\overline{W}$	
$\overline{IOSTB}$	

[MEMO]